Data-Driven Approaches for Indirect Aging Estimation in Power Converters

Ayoub FARAH HASSAN*, Luiz VILLA*, Clement FOUCHER*, Jean ALINEI**
LAAS-CNRS* and OwnTech Technologies**

RESUME - This paper presents an indirect method to estimate the aging of active and passive components in a synchronous buck converter. By monitoring electrical indicators such as efficiency, current ripple, voltage overshoot, and settling time, we demonstrate the ability to detect parameter change resulting from component degradation, including ESR increase, inductance variation, and MOSFET on-resistance ($R_{ds,on}$) rise. A combination of simulation sensitivity analysis, principal component analysis (PCA), and regression models is used to evaluate indicator relevance and build aging estimators. Experimental results confirm that this approach can detect changes in capacitor parameters, validating the possibility of monitoring degradation simply from microcontroller measures.

Mots-clés – Aging estimation, Online monitoring, Buck converter, Electrical indicators.

1. INTRODUCTION

Power converters are essential in modern electrical systems, enabling efficient energy conversion for applications such as renewable energy, electric vehicles, and industrial automation. However, their longevity is a major challenge due to component degradation which affect reliability over time, primarily caused by thermal and electrical stresses [1]. Understanding and estimating this degradation is crucial for improving reliability and minimizing maintenance costs.

Traditionally component aging estimation is generally performed offline and include thermal analysis and direct resistance or capacitance measurements. Active components have a vast literature on failure mechanisms focusing on *bond wire lift-off*, *bond wire heel crack*, and *solder fatigue* [1]. Other methods use accelerated aging techniques. For example, they are used to study the lifespan of capacitors [2]. Other Careful mission profiling using *rainflow counting* enables the calculation of accumulated damage during thermal cycling, allowing for more precise estimates of component lifespan [2].

All these methods are not feasible online. They fail to provide continuous real-time data, which blocks monitoring of converter health *in situ* [3]. There is a clear need for innovative approaches that can translate online indirect data into meaningful indicators of component health [3].

The objective of this research is to address this gap by developing a method for estimating component aging through indirect electrical measurements. The proposed method is designed to be compatible with real-time, embedded monitoring using standard microcontroller peripherals.

2. METHODOLOGY

This work studies multiple electrical precursors and tries to correlate them to estimate aging.

A synchronous buck converter is used as a case study. Its components are shown in Figure 1. The diagram outlines in green the elements that are subject to aging. We can divide them in three main components : The MOSFETs, the capacitor and the inductor.

The red elements are the measurement variables which can be easily acquired by the embedded sensors of the board and will be studied in this work : the current in the inductor (i_{out}) and the capacitor voltage (v_{out})

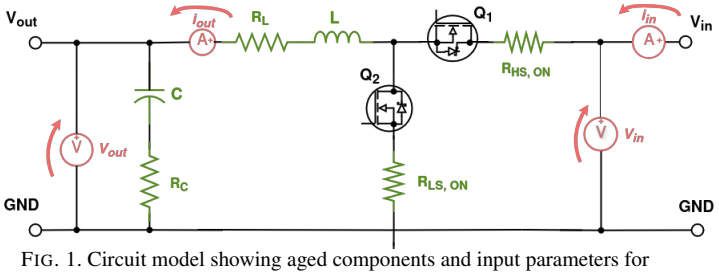

FIG. 1. Circuit model showing aged components and input parameters for analysis. The aged components are marked in green, while the measurement is in red.

2.1. *Analysed Components*

The components considered in this study are those whose electrical characteristics are most affected by aging. This includes the MOSFETs, the output capacitor, and the inductor.

Each of these elements have not only a nominal value (e.g., capacitance, inductance, or gate-source voltage) but also parasitic effects such as the ESR (Equivalent Series Resistance) in capacitors, or parasitic resistance in MOSFETs and inductors.

Over time, aging leads to parameter drifts of these nominal and parasitic components.

2.1.1. *Capacitor*

As discussed in [4], the main cause of the electrolytic capacitor degradation is due to vaporization of electrolytes. Several conditions can lead to this such as High voltage and ripple currents, mechanical vibration and transients. The degradation is therefore linked with an increase in ESR and the decrease in the capacitance overtime. Both [5], [6] present a study on accelerating the degradation of capacitors and that the capacitor value decrease at a slower rate than the ESR value. These parameter shifts directly affect the converter's dynamic response leading to more pronounced overshoots, and the overall damping of the LC filter is altered.

2.1.2. *MOSFETs*

According to [7], thermal aging in MOSFETs comes from mechanical stress in the die area, where the silicon is soldered to the copper substrate. Due to the mismatch in coefficients of thermal expansion (CTE) between the different materials, temperature variation creates uneven expansion and retractions leading to a crack in the solder. This leads to a rise of the junction temperature which causes an increase in the value of the ON resistance $R_{\mathrm{ds,on}}$. The increase in $R_{\mathrm{ds,on}}$ leads to higher conduction losses, reduced efficiency, and more thermal stress, reinforcing the degradation and creating a positive feedback loop. At the control level, a higher duty cycle is required to maintain the same output voltage, compensating for the increased voltage drop across the

MOSFET.

2.1.3. *Inductor*

A study is made for surface mounted inductors in [8], focusing on the effect of thermal aging. The high temperature can damage the insulation between ferromagnetic core particles causing an increase in the eddy current and core losses. Some of the symptoms are higher power losses, increase in self-heating and electromagnetic interference. The study shows that there is variation in the inductor value, but not as significant as the decrease in the quality factor Q related to the inductor and DC resistance value. This indicates that the series resistance R_L is the most affected parameter during inductor aging. A variation in L results in the reducing of the filtering effectiveness, higher current ripple, and weaker damping, while an increase in R_L can affect the power loss. All of which impact the system's stability and efficiency.

2.2. *Excitation Setup*

In order to capture the behavior of aged components, two types of measurement are required : one to get the steady-state values, and another focusing on dynamic response of the system.

The converter's excitation is conducted in two distinct phases as shown in Figure 2.

Closed-Loop phase in blue (PID-controlled phase) : First the converter operates using a PID controller to regulate its output voltage to half of the input. The idea is to compare steady-state values of the converter when the output voltage held at a fixed value. During this phase, we record parameters such as average output voltage/current, duty-cycle used to maintain the output voltage, input/output power and efficiency.

Open-Loop Phase (Step Response Phase) : On the second phase, the converter operates at a constant duty cycle of 50% and is subjected to a step change from 50% to 70% and then returned to 50%. The system's transient is then analysed to extract data such as natural frequency (ω_n), overshoot, settling time and quality factor (Q). These parameters should be sensible to changes in passive components like inductor and capacitor.

These two analyses allow us to record all the necessary information to detect a degradation in the components, with a simplicity of implementation since all of the measurement can be done via the microcontroller and then send to a computer for an analysis or even done in the microcontroller for real-time embedded monitoring.

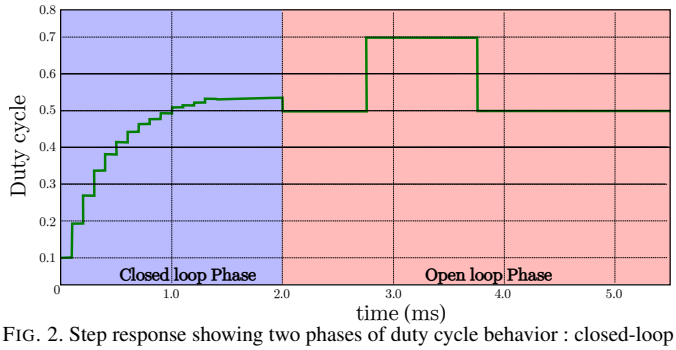

FIG. 2. Step response showing two phases of duty cycle behavior : closed-loop control (stabilization) and open-loop control (step changes).

2.2.1. *Measurement*

As shown in Figure 1 we have placed sensors in the input and output stages to get all the current and voltage measurement needed. This provides us with the needed information for computing the efficiency, and the average output power. This can also help us to measure the current ripple and voltage dynamic response. The synchronous buck is being controlled by microcontroller unit (MCU), for generating the PWM and getting measurements from the sensors. However, the control task of a microcontroller is generally using a control task loop which runs at a few tens of kilohertz. On the other hand, the current ripple has the same frequency as the switching frequency which is in the hundreds of kilohertz. Thus the Nyquist-Shannon criterion is not respected, and direct sampling of the ripple is not possible. To solve this problem, we use a shifted sampling method as illustrated in Figure 3.

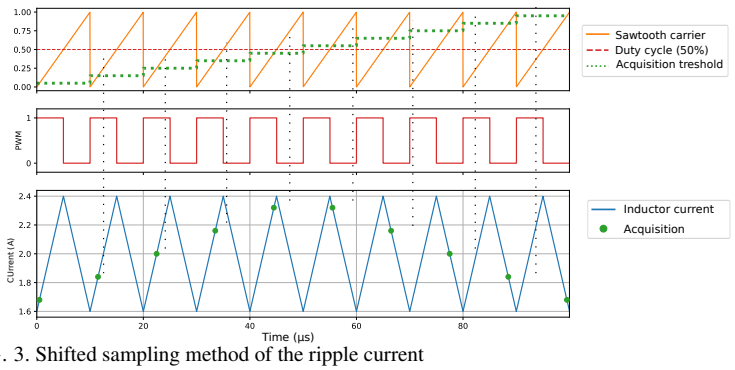

FIG. 3. Shifted sampling method of the ripple current

In steady state, the acquisition instant is updated periodically, allowing us to capture different values of the ripple waveform through multiple cycles. We can then reconstruct the full waveform offline. Having the full waveform allows us to compute the current slopes and detect any anomalies in the inductor behavior such as change in the ripple shape or assymetry.

In practice, this shifting occurs at the control period rate. For clarity purposes, the illustration in Figure 3 the method is applied at the switching frequency. However, during a step response analysis with fast transient, the system dynamics might be too fast to be acquired correctly with only the control task. Software-based acquisition is then not enough, and a hardware-triggered acquisition strategy is preferable.

To do so, the MCU's analog-to-digital converter (ADC) is configured to automatically sample every three switching periods, and the values are transferred to a memory buffer via direct memory access (DMA).

This process is done independantly of the control loop execution and CPU intervention and is generally used in MCU when a higher acquisition rate is wished [9]. Althought we cannot update the acquistion instant at the switching frequency, it's not a problem in this case since the mean value is enough to get the full dynamic response.

2.3. *Aging indicators*

To estimate aging, we monitor several electrical indicators. These indicators will be evaluated to provide information on how the converter ages over time. All of these data are extracted from the measurements in the closed-loop and open-loop steps.

- **Input power and output power** : A variation in the power can suggest an increase in switching and conduction loss for the MOSFETs, and change in the parasitic resistance in capacitor and inductor.
- **Efficiency** : We expect a decrease in efficiency as the degradation progresses due to increased power loss.
- **Closed-loop duty cycle** : During the closed-loop phase, due to the increase of parasitic resistance there will be more voltage drop, thus requiring a higher duty cycle to maintain a fixed voltage reference.
- **Step Response time to 5%** : This is the time required for the output voltage to settle within 5% of its final value. This value depends on the system dynamic response which is higly correlated to a change in L and C.
- **Output voltage overshoot** : A high overshoot during step response analysis suggests a change in either C or L since

TABLEAU 1. summary of the test done, recorded indicators and analysed components

Test Phase	Indicator	Analysed Components
Closed-loop	Input/output power	MOSFETs ($R_{\mathrm{ds,on}}$), Inductor (R_L), ESR
	Efficiency	MOSFETs ($R_{\mathrm{ds,on}}$), Inductor (R_L), ESR
	Duty cycle	MOSFETs ($R_{\mathrm{ds,on}}$), Inductor (R_L)
Open-loop	Step-response to 5%	Capacitor (C, ESR), Inductor (L)
	Output voltage overshoot	Capacitor (C, ESR), Inductor (L)
	Current ripple at 50%	Inductor (L)
	Natural frequency, Q	Capacitor (C, ESR), Inductor (L)

a variation of their values can reduce the damping.

— **Current ripple at 50%** : Current ripple and current slope depend only on the inductor value, it can be an important parameter to distinguish changes from the capacitor and the inductor.

— **Natural frequency** (ω_n) : This is the natural frequency as defined by the LC filter, this frequency shift with variations in inductance and capacitor.

— **Quality factor (Q)** : The quality factor reflects how well the system is damped, so it depends directly on the C, L and also on parasitic resistor.

The natural frequency and the quality factor can be extracted by feeding the measured values to an identification toolbox such as the one provided by MATLAB. However for simplicity we can also work with time-domain parameters such as the settling time and overshoot since they convey the same kind of information (speed and damping).

This paper proposes a simulation study of these indicators to generate data that will be then analyzed to determine which indicator is linked to the degradation of each electrical parameter. We will use the data to fit a model and then aim to estimate the aging of the different parameters using a test dataset.

2.4. *Simulation Setup*

This work uses a Simulink Simscape model available here.

We conduct two sets of simulations to analyze component aging :

Sensitivity Analysis : The first set of simulations focuses on analyzing the sensitivity of the indicators to variations in individual component parameters.

Linear Degradation of Individual Components : The second set of simulations involves progressively degrading one component at a time while keeping all others constant.

Linear Degradation of All Components : The final set of simulations degrades all components simultaneously. These data will be used as a test dataset to verify the fit done with the individual datasets.

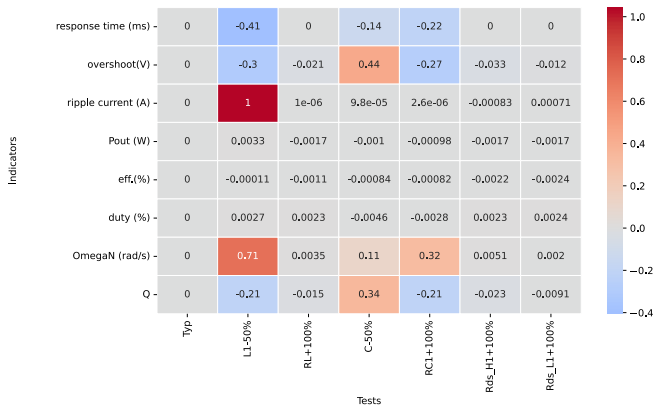

FIG. 4. Heatmap showing the sensibility of the different indicators.

3. SIMULATION RESULTS AND DATA ANALYSIS

This section analyzes the data via different methods including principal component analysis (PCA), linear regression with RMSE, and a heatmap of the regression coefficients.

The sensitivity analysis was performed by comparing the values of the indicators obtained with typical component parameter values and maximum component variation. By testing with maximum variation, we can determine which indicator is most sensitive and by how much.

The sensitivity analysis results were normalized then subtracted from 1, giving figure 4. Values close to zero mean no notable change compared to reference conditions.

This analysis shows that the overshoot is very sensitive to changes in capacitance, inductance and parasitic resistances. The other indicators were not as sensitive to the variations.

PCA was used to reduce dataset dimensionality and identify key performance indicators. The first three principal components captured most of the variance, highlighting metrics such as settling time, overshoot, and efficiency.

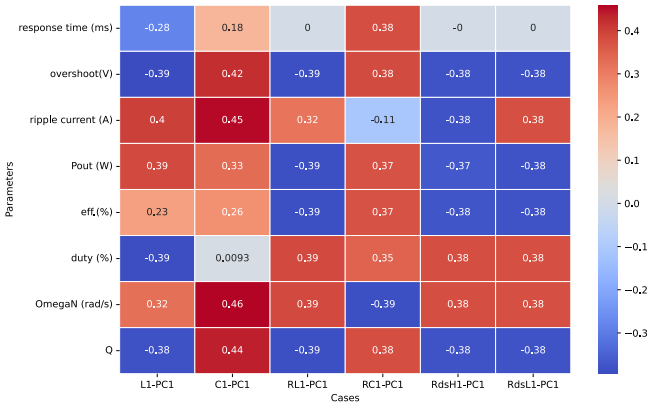

FIG. 5. Weights of each indicator for PC1 in all components

Figure 5 illustrates that the weights associated with the PC1 for all the parameters. It shows that by combining multiple indicators, it is possible to explain the data. It shows that $R_{DS_{ON}}$ is mostly explained by the duty cycle and ripple current.

Linear regression was applied to model the relationship between the performance indicators and the degradation of each component. The root mean square error (RMSE) was calculated for each parameter to assess the accuracy of the regression models as shown in Table 2.

These results show that one single fit technique does not work well for all paremeters.

4. EXPERIMENTAL RESULTS

4.1. *Experimental setup*

To check if the microcontroller is capable of detecting variations in component values, an experimental test was conducted on a two-leg buck converter. The schematic of the tested converter is shown in Figure 6.

TABLEAU 2. Root Mean Square Error (RMSE) for each regression model across different parameters.

Model	L1 μH	C1 μF	RL1 $m\Omega$	RC1 $m\Omega$	RdsH1 $m\Omega$	RdsL1 $m\Omega$
Linear	4.05	65.2	276	13900	664	2590
Lasso	5.35	6.68	5.67	50.7	989	36.4
Poly	10.1	74.8	1250	7440	1800	8320
SVR	6.02	7.24	5.53	18.6	5.74	5.74
GPR	2.91	55.3	11.1	823	360	39.9

This test focuses on identifying changes in the output electrolytic capacitor. Two configurations were compared :

— **C_low1** : capacitance of 47 µF with an ESR of 0.7 Ω
— **C_low2** : capacitance of 33 µF with an ESR of 1.3 Ω

The other components such as the inductor and the MOSFETs are identical between the two legs. The switching frequency f_{sw} is 200kHz and the input voltage is 25V. The two legs are connected to a 7 Ohm resistive load.

TABLEAU 3. Experimental setup parameters

Component	Value / Specification
Inductor	33 µH, DCR = 18 mΩ
MOSFETs	$V_{DS} = 150$ V, $R_{ds(on)} = 16$ mΩ
$C_{1\ low}$	47 µF, ESR = 0.7 Ω
$C_{2\ low}$	33 µF, ESR = 1.3 Ω
Input voltage	25 V
Resistive load	7 Ω
Switching frequency	200 kHz
Control loop period	100 µs

The objective is to determine whether such changes in both capacitance and equivalent series resistance can be detected through the electrical indicators recorded by the microcontroller.

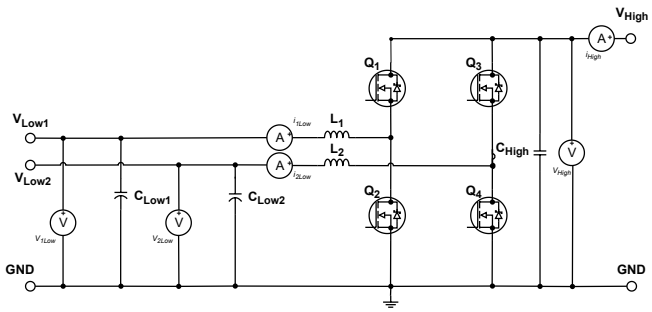

FIG. 6. Schematic of the buck for the test

The power electronics stage is controlled by an STM32G474RE microcontroller, which includes the necessary peripherals for data acquisition and PWM generation to drive the two-leg buck converter.

As illustrated in Figure 7, the microcontroller acquires the necessary analog values from the power circuit and generates the PWM reference signal to control the buck converter. Once the test is complete, the MCU transmits all the recorded digital data to a PC for post-processing. The analysis can be performed using either MATLAB or Python.

An intermediate IoT device could also be used to wirelessly transmit the data from the microcontroller to the PC, enabling remote data collection and monitoring.

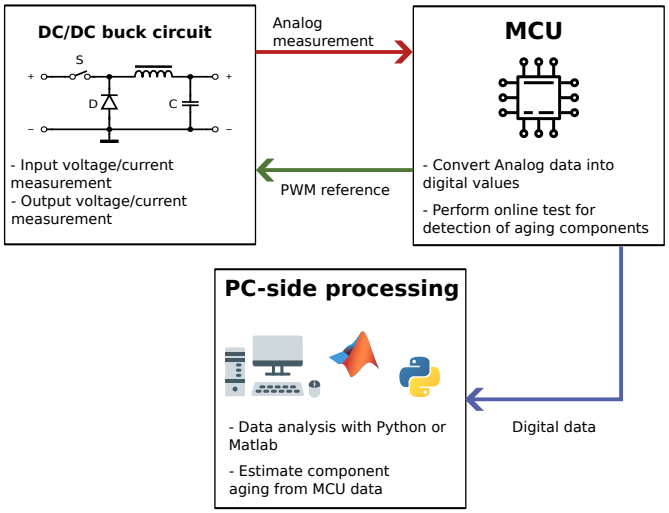

FIG. 7. Analysis process

4.2. *Experimental results*

The experimental tests were first conducted using the leg equipped with **C_low1**, followed by a second set of tests using **C_low2**. To ensure thermal consistency, power is supplied to the leg and the system is allowed to stabilize until the high-side MOSFETs reach a temperature of 35°C, ensuring that both configurations operate under similar thermal conditions.

Once the desired temperature is reached, the step response test described in Figure 2 is performed. The relevant electrical measurements are collected by the microcontroller and transmitted to the computer for analysis. This procedure is repeated 5 times, and the averaged results are summarized in Table 4.

TABLEAU 4. Comparison of measured indicators for C_low1 and C_low2

Indicator	C_low1	C_low2	Normalized sensitivity
Overshoot	9.70 %	13.00 %	0.340
Settling time	150 µs	170 µs	0.133
Output power	21.5 W	22.9 W	0.065
Current ripple	403 mA	392 mA	-0.022

From the results presented in Table 4, we observe an impact on the overshoot. This effect is also illustrated in Figure 8, where the increase is relatively small, but still detectable by the microcontroller.

As highlighted in the sensitivity analysis of Figure 4, a decrease in the capacitance tends to increase the overshoot, while a higher ESR contributes to the damping of the system. This explains the modest increase in overshoot observed with C_LOW2 compared to C_LOW1.

A small increase in output power is observed with C_{low2}, which is consistent with the expected losses caused by the higher ESR.

Finally, the ripple current remains similar between both configurations, which is expected, since the inductor is the only component controlling current ripple.

Experimentally, we used a capacitor whose parameters differ by approximately $C_{-30\%}$ and $ESR_{+90\%}$ compared to the standard case (C_{low1}). This degradation is close to the sensitivity study case of $C_{-50\%}$, $ESR_{+100\%}$ used in the simulation. As shown in Figure 9, the overshoot remains of identic magnitude between both cases, highlighting the consistency of the indicator in simulated and experimental result.

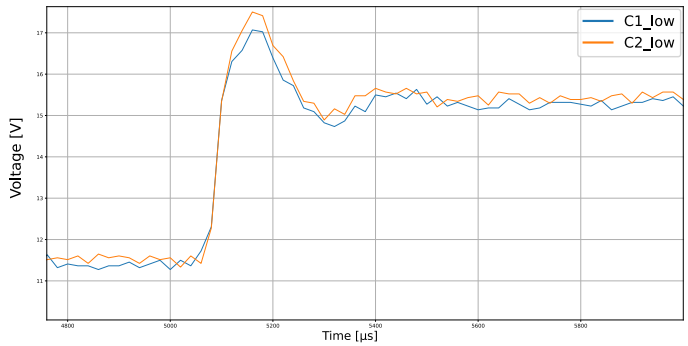

FIG. 8. Step response analysis for C_low1 and C_low2

However, while the simulation suggests a shorter rise time under capacitor degradation, the experimental results show a slower response. This apparent contradiction may be due to two effects : first, the larger overshoot observed experimentally could result in a longer settling time; second, the limited sampling resolution of the microcontroller may impact the accuracy of rise time estimation, especially at the 5% threshold. A finer acquisition, or the use of hardware-triggered sampling at higher frequency, could help clarify this aspect in future tests.

It would be also relevant to test a broader range of degraded capacitor values, as well as other components such as inductors and MOSFETs. This would enable the construction of a sufficiently large experimental dataset to apply regression techniques directly to real measurements, with the aim of estimating component values and detect failures through continuous monitoring.

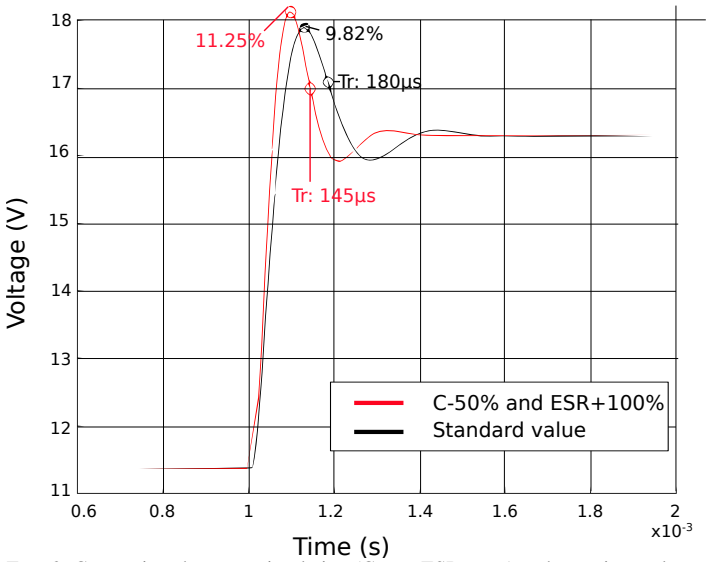

FIG. 9. Comparison between simulation ($C_{-50\%}$, $ESR_{+100\%}$) and experimental step response.

5. CONCLUSION

This work presents a methodology to estimate the aging of components in a synchronous buck converter using only electrical indicators accessible via microcontroller. By analyzing both steady-state and transient behaviors, we identified several measurable parameters, that are sensitive to variations in parasitic and nominal component values.

A complete simulation campaign was conducted to evaluate indicator sensitivity and fit regression models. Principal component analysis revealed that combining multiple indicators enhances degradation detection accuracy. Experimental validation confirmed that the proposed method is capable of detecting changes in capacitor parameters, even with simple acquisition hardware like MCU's ADC.

Future work will focus on gathering datasets from aged power electronic boards in order to define failure thresholds for component lifetime monitoring.

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