Specifications and Design of a DC-DC Converter for Decentralized DC Microgrids in Rural Africa

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ABSTRACT – DC microgrids are an essential tool to achieve universal electricity access, especially in rural zones of Sub-Saharan Africa or South-East Asia. In particular, decentralized DC microgrids, where storage and production resources are disseminated over the whole microgrid, are gaining momentum in the rural electrification sector. However, such microgrid topology is entirely based on power electronic structures and their associated controls. The design of these power electronic converters must therefore be thought with respect to the targeted application, which is however open to changes. In addition, the costs, the modularity of usage and services and the ease of use of the converters are the main drivers to focus on during the design stage in comparison to conventional designs where volume, weight and efficiency are often favored. This paper draws precisely the converter specifications adapted to DC microgrids with decentralized production and storage, and then presents an exhaustive search algorithm to optimize the number of arms and the microgrid DC bus voltage with respect to the cost of the converter. A hardware prototype is finally presented.

Keywords – Nanogrid, Microgrid, Rural electrification, DC-DC converter.

1. INTRODUCTION

Nowadays, almost one billion people are struggling because of limited access to electricity despite the United Nations (UN) Sustainable Development Goals of ensuring universal access to reliable and modern energy services by 2030. This mostly concerns rural places in Sub-Saharan Africa or South-east Asia, where abundant resources in solar power are available and no national electricity infrastructures are usually developed mainly because of high upfront connection costs [1, 2, 3].
Following the observation that conventional methods to tackle rural electrification (such as national grid extension, centralized minigrids and Solar Home Systems) have been continuously failing in the past decades [1, 2, 3], Nanoé, a French-Malagasy social company created in 2017 [4], develops and experiments in the North of Madagascar a novel Lateral Electrification model based on renewable energies, digital technologies and local entrepreneurship [3]. Technologically wise, the Lateral Electrification model follows the swarm electrification concept of progressive building of power infrastructures in a bottom-up manner [5], enabling modularity and scalability, by nimbly and progressively extending the energy services delivered to the end-users (from Tier 1 to Tier 5 as defined by the multi-tier framework of the UN [6]) through the diffusion and the aggregation of basic smart power units (named nanogrids) regrouping solar power generation, storage and distribution as described in Fig. 1.
Therefore, in collaboration with G2Elab, Nanoé is developing DC microgrids with decentralized production and storage to enable the second step of its electrification model. However, such microgrids entirely rely on power electronic structures and their associated local controls [1, 7, 8, 9]. As the application for which the converter is designed is still in development and open to modifications, it is of interest to study how the microgrid application and the converter specifications are intertwined. In particular, grid services performed by the converter for the microgrid could definitely facilitate the operation of the proposed microgrid. This approach is drastically different from traditional works on converter design for power systems, where the converter specifications are usually very well framed by the power system applications, strongly limiting the possibilities that power electronic could bring to power systems.
This paper details in Section 2 the converter specifications needed for a decentralized DC microgrid application. Then, in Section 3, an exhaustive search algorithm is presented to cost optimize the converter with respect to the application. Finally, Section 4 shows the hardware realization of the proposed converter.

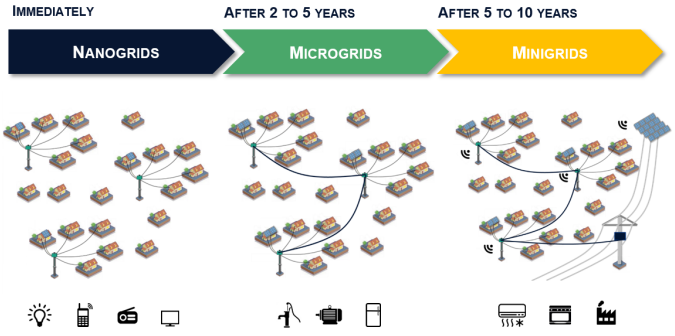

FIG. 1. Progressive building of electric infrastructures.

2. DC-DC INTERLEAVED CONVERTER

2.1. *Microgrids with Decentralized Production and Storage*

The proposed microgrid is designed to interconnect all 12 or 24 V DC nanogrids within a close area to a common DC bus. In addition, communal loads operating at 24 or 48 V up to 1.5 kW, such as agro-processing machines, can be connected to the common DC bus. The main element of the microgrid is the interconnection module, which can either interface a nanogrid or a communal load to the common DC bus (respectively in red and blue in Fig. 2). Each interconnection module is controlled by a decentralized and communication-free algorithm, presented in [7], and developed to control whether the nanogrid must inject or absorb current from the microgrid, based on the nanogrid State-of-Charge (SoC) and the common DC bus magnitude.

2.2. *Converter Specifications*

First of all, the interconnection module interconnects a 12 or 24 V DC nanogrid to a microgrid DC bus whose voltage V_{bus} is below 120 V DC (to stay below the extra-low DC voltage threshold). Staying under 120 V DC enables to suppress the need for a galvanic isolation between the input and the output of the converter, as there is no safety concerns for end-users even if they are by accident in contact with the output voltage. In addi-

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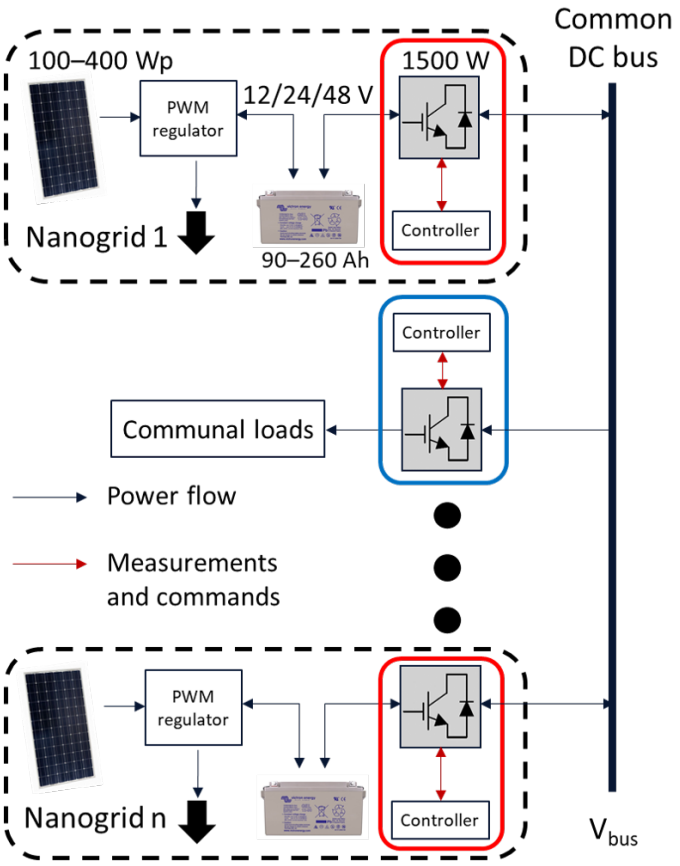

FIG. 2. Topology of the proposed microgrid.

tion, power flows are bidirectional as the nanogrid can inject or absorb current from the microgrid DC bus. Therefore, as a first step, a bidirectional non-isolated boost function is needed for the interconnection module. However, the optimal output voltage has yet to be determined. The microgrid could operate between 60 to 96 V. Lower and higher voltages are too close respectively to the maximal communal load voltage and to the extra low voltage threshold of 120 V. Thus, the DC bus voltage level is left as an optimisation variable for the exhaustive search algorithm presented in Section 3.

On the other hand, converter design for low-voltage medium power applications usually implies relatively high current rating of the converter. To reduce current in the boost power inductor, multiple phases can be put in parallel in an interleaved boost converter. This also enables to diminish output voltage and input current ripple without increasing the size of the passive components and therefore to reduce overall costs. The output voltage ripple reduction is of particular importance for the control algorithm of the interconnection module, based on the DC bus voltage. Multiple arms also enable modularity and can increase efficiency over a large power range (only one arm used at low power to decrease switching losses for instance). In addition, it reduces the current per arm for a specified power rating, which eases the choice of the power inductors, the rating of the mosfets and the thermal management of the entire converter. However, the optimal number of arms of the interconnection module has yet to be determined and is left as an optimisation variable in the exhaustive search algorithm.

Therefore, in line with the main objective of this converter design to minimise cost, a classical synchronous interleaved boost topology can be chosen for the interconnection module. However, to operate safely and satisfyingly a DC microgrid with decentralized production and storage, start-up and protection features must be implemented. Usually, costly electromechanical components such as circuit breakers for protection or pre-charge relays for start-up are installed on the microgrid to perform those necessary functions. It is then economically interesting to include those features directly within the interconnection module to suppress these costly (and often less reliable) devices.

Firstly, at start-up of the microgrid, the first interconnection module to launch must charge all the DC bus and the associated high capacitance (composed of the output capacitors of all the interconnection modules) to the nominal voltage of the microgrid. If only composed of a boost structure, the first interconnection module to launch would directly apply its input voltage on the DC bus (through the body diode of the high-side mosfet), charging instantly the DC bus capacitors to its input voltage, generating a very large inrush current only limited by the cable resistances. A buck-boost topology, as shown in Fig. 3, enables to follow a start-up procedure, presented in [9], where the DC bus is firstly charged to a voltage close to the nanogrid voltage, with the interconnection module in buck operation, before switching to boost operation for normal power exchange.

Secondly, if only composed of a boost structure, the interconnection module would always connect the nanogrid to the microgrid DC bus, through the high-side mosfet body diodes (Q4 and Q8 in Fig. 3). Yet, short circuits on the DC bus or undervoltage events, where the voltage would drop to a lower value than the nanogrid voltage, could happen. In that case, a boost structure would fail to manage such events due to the presence of the high-side mosfet body diodes whereas a buck-boost converter could switch to buck conversion or completely disconnect the nanogrid to the microgrid by opening the high-side buck mosfets to overcome short-circuits or undervoltage events. Overall, adding a buck structure to the interconnection module enables to enhance its protection features as it can then completely disconnect the nanogrid to the microgrid, in case of voltage or current exceeding predefined limits, and offer a free-wheel path to the current in the power inductors and thus limit the constraints on the interface mosfets.

Furthermore, due to the particular expectations of this work of quickly confronting the proposed solution to the field, the converter must offer ease of design and conception. Therefore, only off-the-shelf components can be used. This constraint impedes to use only two boost arms as 15 A off-the-shelf inductors of the needed inductance value are very difficult to find. Similarly, the majority of the components must be straightforward to assemble on the PCB, to enable local mounting in Madagascar and increase reparability and disassembling possibilities.

In addition, the interconnection module must offer a high level of modularity in three areas :

- modularity of usage, so that one hardware design only (for production costs and logistic reasons) enables to interconnect classic nanogrids but also communal loads and nanogrids without batteries to the microgrid DC bus,
- modularity of power, to adapt to the different nanogrid and communal load sizes,
- modularity of voltage, to be able to operate with 12, 24 or 48 V DC on the low voltage side and a varying output voltage centered around V_{bus} with a $\pm$ 10% range.

Finally, in terms of power converter rating, in line with a power exchange limit with the microgrid set at a tenth of the battery size (i.e. at most 26 A for the biggest nanogrid) and with maximum communal load power rating (i.e. 1.5 kW at 48 V), a current rating of 30 A on the low voltage side is chosen for the interconnection module. However, one power sizing would incur useless costs for small nanogrids or small communal loads by installing the full power whereas it would never be used. On the contrary, multiple power levels would enable to adapt better to the nanogrid or communal load size by fitting the interconnection module rating to their size. This is also consistent with the interleaved structure of the interconnection module. An interconnection module composed of a command card and multiple power cards (at least two) would enable to distribute the different arms of the interleaved structure on different power cards and to mount only the necessary power cards with respect to

the power needed. Realistically, two, three or four power levels appear possible (hence with 7.5 A, 10 A, 15 A respectively per power card). Therefore, a design with five boost arms is also excluded from this study as five arms are not divisible by two, three or four, impeding power modularity.
The converter specifications are summarised in Table 1, with the optimal number of boost arms and the DC output voltage indicated in red as they are yet to be determined by the exhaustive search algorithm. The switching frequency of the interconnection module is fixed at 50 kHz as a compromise between the complexity of design, the reduction of the size of passive elements, EMC and the switching losses. This switching frequency is also consistent with micro-controller capabilities and the fine tuning of the duty cycle needed to achieve proper current regulation. In addition, maximum levels of output voltage and input current ripple (respectively at the output and input of the switching cell within the dashed blue line in Fig. 3, before the output filter in dashed red line) are chosen to obtain a stable enough output voltage measurement for the proper implementation of the proposed control algorithm of the interconnection module.

TABLE 1. Interconnection module specifications.

Category	Symbol	Details
Switching frequency	F	50 kHz
Input voltage (min/max)	V_{bat}	12 V (10.5 to 14.5 V) 24 V (21 to 29 V) 48 V (45 to 51 V)
Output voltage	V_{bus}	60 V, 72 V, 84 V, 96 V
Number of boost arms	q	3, 4 or 6
Power modularity	N_P	2 to 4 levels
Modularity of usage	–	Nanogrids Communal loads bus
Number of buck arms	N_B	1 to 6
Output voltage ripple	ΔV_S	0.5 V
Input current ripple	ΔI_T	1 A
Current rating	I_{conv}	30 A
Temperature elevation	ΔT_{max}	50 °C

3. DESIGN METHODOLOGY

3.1. *Theoretical Study*

An example of the proposed interleaved bidirectional buck-boost converter is shown in Fig. 3, where only two arms are represented for the sake of clarity. During normal operation, the high-side buck mosfets (Q1, Q5) are always closed whereas the low-side buck mosfets (Q2, Q6) are always open. The duty cycle α is defined for the boost low-side mosfets Q3 ans Q7. In an interleaved converter with q arms, the switching commands of the boost arms are phase-shifted between them by T/q.

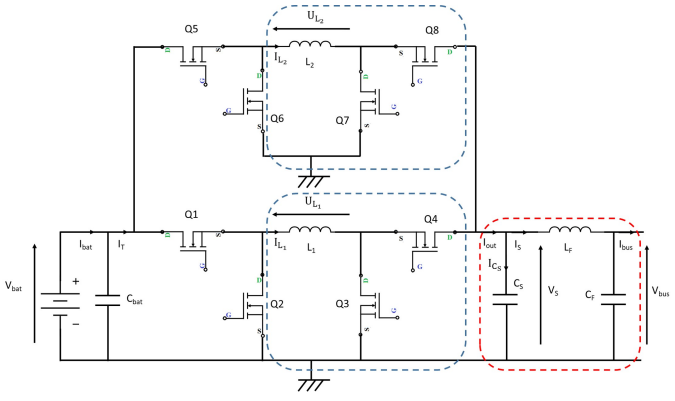

FIG. 3. Interleaved two-arm buck-boost converter.

The formula linking the input voltage V_{bat} to the output voltage V_S before the output filter is given in equation 1.

$$V_S = \frac{V_{bat}}{1-\alpha} \tag{1}$$

To size the passive elements of a converter, i.e. its power inductors and its output capacitors, the formula evaluating the input current I_T and output voltage V_S ripple must be determined. The general formulas for q number of arms is given in equations 2 and 3, with α_{eq} the integer part of the αq product. Note that I_T and V_S might be approximated to I_{bat} and V_{bus} as in average the input capacitor current and the voltage across the output filter inductor are equal to 0 in steady-state.

$$\Delta I_T = \frac{qV_{bat}}{LF\cdot(1-\alpha)}\cdot(\alpha-\frac{\alpha_{eq}}{q})(\frac{\alpha_{eq}+1}{q}-\alpha) \tag{2}$$

$$\Delta V_S = \frac{I_{bat}}{C_S F}\cdot(\alpha-\frac{\alpha_{eq}}{q})\cdot(\frac{\alpha_{eq}+1}{q}-\alpha) \tag{3}$$

3.2. *Exhaustive Search Algorithm*

The exhaustive search algorithm aims at determining the technico-economic optimal design of the interleaved DC-DC converter presented above. The DC bus voltage (i.e. V_S before the output filter or V_{bus} after as indicated in Fig. 3) and the number of arms q are the optimisation variables, while the objective is the minimisation of the switching cells cost. Only the cost of the boost switching cells are considered, including the power inductors, the output cell capacitors, the boost mosfets, their associated drivers and thermal heatsinks and the arm current sensors. The input and output filters are omitted from this optimisation study.

3.2.1. *Costs Modelling and Mosfet Losses Evaluation*

Cost modelling for power inductors is definitely complicated. A first and straightforward method to implement would be to derive general linear formulas linking the overall costs to the value of the inductance (L) and its current rating (I) through the analysis of manufacturer catalogs. However, despite numerous attempts, no general formulas were found to be satisfying even by trying to interpolate with respect to I^2 or LI^2, as the interpolation coefficient was always below 0.9. Similarly, a method based on the evaluation of materials costs through the sizing of its magnetic core and copper wires fails. Indeed, power inductors are labor-intensive as confirmed by [10] and therefore a major part of their costs are associated with the cost of labor, which tends to vary a lot depending on the quantities and location of the manufacturing process. Therefore, the final chosen method is based on manufacturer catalog costs by considering discrete values for the power inductors. This method has the huge drawback to depend on inductor data set, which is often difficult and time-consuming to gather.
On the opposite to power inductors, general linear formulas can be estimated for film capacitors. Their costs depend mainly on the capacitor value and much less on capacitor voltage, especially when the application voltage varies by little. Interpolation coefficients over 0.99 are obtained for instance for the B32520 series from the manufacturer EPCOS. This is confirmed in [10] where linear formulas are found for film capacitors with respect to the rated capacitance and the voltage rating (although with a much smaller coefficient for the voltage rating than for the capacitance). In addition, these output capacitors can be placed in parallel to obtain precisely the needed capacitor value. This is even beneficial as it reduces the nominal current within each capacitor as well as the total ESR (Equivalent Series Resistance) of the output capacitors.

Thirdly, the selection of the power mosfets depends principally on their voltage rating, i.e. the voltage they are able to withstand, their on-state resistance and their switching characteristics. Due to switching overvoltage and for safety margin, the mosfet voltage rating V_{DS} must ensure the following criteria with respect to the microgrid DC bus voltage (at most equal to $1.1 \cdot V_{bus}$) . This designer rule is based on manufacturer feedback.

$$1.1 \cdot V_{bus} \leq 0.8 \cdot V_{DS} - 10 \quad (4)$$

In addition, all the power mosfets considered in this design must enable to obtain power mosfet losses below 2 W to ease the choice of the heatsink. Mosfet losses P_{loss} are composed of two main parts :

- conduction losses P_{cond}, due to the current flowing in the component when closed, mainly linked to R_{DS},
- switching losses P_{sw}, due to transitions between closed and open states, and linked to the switching characteristics.

Once a mosfet is selected in the exhaustive search algorithm, its maximal losses are calculated, and the needed thermal resistance of the heatsink to stay below a 50 °C elevation of the temperature (i.e. ΔT_{max}) is calculated. In this design, using PCB as heatsink is preferred. Therefore, following [11], if the needed thermal resistance R_{th} is above 37 K/W, no heatsink is selected except a PCB copper area around the mosfet. Below 37 K/W, four different heatsinks found after a catalogue search are considered, with increasing prices as the thermal resistance gets lower. When the PCB is used as heatsink, this is considered free as PCB costs are usually very low and as this heatsink method is believed not to expand much the size of the PCB.
Finally, and after a thorough review of available power mosfets on the market, two different types of components have been considered for most voltage ratings, one more expensive but generating less losses, appropriate for a small number of arms, and one less expensive but generating more losses, appropriate for a high number of arms (as the current per arm is then lower). Note that mosfet prices tend to increase significantly for a 150 V voltage caliber in comparison to 120 or 100 V.
To drive the boost power mosfets, a bootstrap component is selected. The drawback of bootstrap component is that they can not assure a duty cycle so that the high-side mosfet is always closed. However, in this application, this is never the case for the boost arms. An extensive review of the different bootstrap components available has set its price around 1 €.
Then, a current sensor is placed in each arm to precisely control each current in order to equally balance the total current. In addition, the current sensors must be bidirectional. The shunt method is not appropriate in this case as a voltage reference must be added to be able to measure bidirectional currents but also because the operational amplifier might not support a 48 V input voltage (in case of a 48 V communal load). Therefore, for ease of design and cost reasons, a Hall effect sensor is selected. Based on an extensive catalog review, its price is set at 3 €.

3.2.2. *Flowchart of the Algorithm*

The exhaustive search algorithm is a heuristic method based on designer-defined rules [12] which explores all possible (V_S, q) combinations to determine the associated cost of the switching cells. The input voltage V_{bat}, either centered around 12 or 24 V, varies as indicated in Table 1 and the output voltage varies by ± 10% centered around V_S in accordance to the operation of the proposed microgrid. To consider the worst case, this study is performed with a battery current set at the maximal power rating of the converter I_{conv}, i.e. 30 A. Firstly, for a given (V_S, q) combination, the range of the duty cycle α is determined both for a 12 V or a 24 V battery as well as the maximal current per arm (i.e. $I_{arm} = \frac{30}{q}$). Then, based on equations 2 and 3, the values of the power inductor and the output capacitor with their associated costs are derived. Simultaneously, the mosfets, mosfet drivers and current sensors are selected and their costs determined. Heatsinks are then selected to keep the elevation of temperature inferior or equal to 50 °C. The total cost can finally be summed up for this (V_S, q) combination. The number of arms q or the DC bus voltage V_S is then modified until all possible combinations are evaluated. The flowchart of the exhaustive search algorithm is illustrated in Fig. 4.

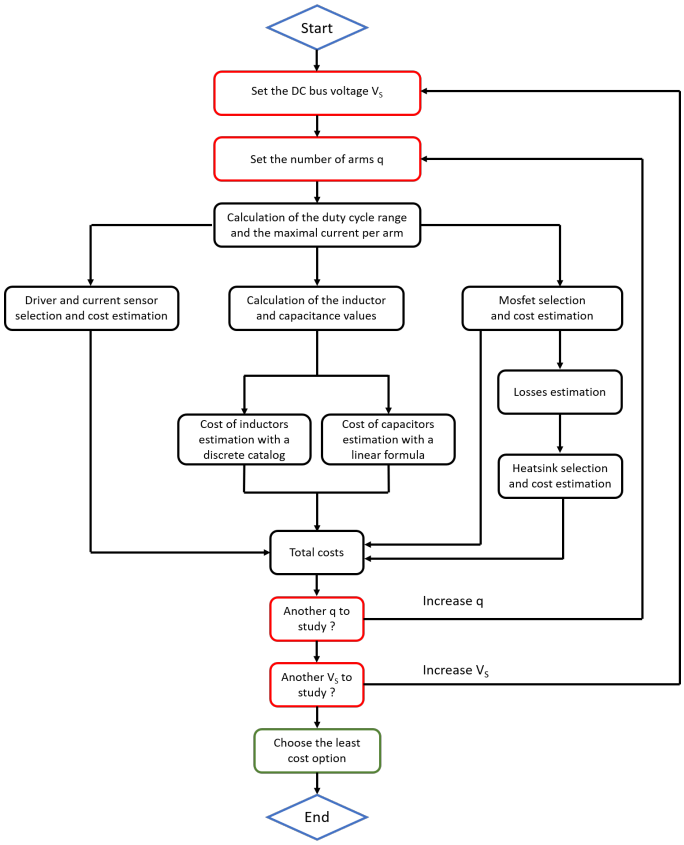

FIG. 4. Flowchart of the exhaustive search algorithm.

3.3. *Results*

The results of the exhaustive search algorithm are shown in Table 2, where the total costs for different (V_S, q) combinations are indicated both for a 12 V (in red) or 24 V (in black) battery input voltage. The cost differences between the 12 and 24 V configurations come mostly from the inductor costs, which are higher in the 12 V configuration because the duty cycle α range is often less favorable for the input current ripple in the 12 V configuration than in the 24 V one, as confirmed in Fig. 5 showing the range of inductor and capacitor values for all possible duty cycles. In addition, this shows that the inductor and capacitor values both decrease with the number of arms and that the inductor value tends to increase with the DC bus voltage, on the contrary to the output capacitor quite stable with respect to V_{bus}. Note that the inductor and capacitor values are sometime equal to 0, as the duty cycle α might take special values for which equations 2 and 3 are equal to 0. However, in most cases, as the input and output voltage of the switching cell both vary, the duty cycle range of operation unfortunately spans most of the possible values in equations 2 and 3.

TABLE 2. Cost (in €) of the switching cells for different (V_S, q) combinations.

q \ V_S	60 V	72 V	84 V	96 V
3	75.9/63.3	76.9/72	81.1/80.3	91.8/91.6
4	73/70.7	73.3/70.7	83.2/80.3	83.2/82.5
6	85/85	84.9/85	99.2/99.4	109.8/99.4

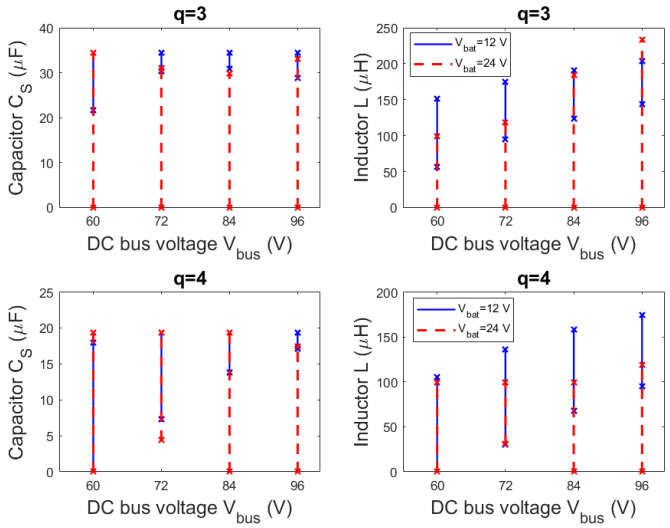

FIG. 5. Inductor and capacitor values depending on V_S, q and α.

The Table enables to affirm that configurations with three or four arms and with an output voltage at 60 V or 72 V are preferred. Indeed, for V_{bus} equal to 84 or 96 V and for a given number of arms, the mosfet costs tend to increase a lot due to the need of a higher voltage rating. The increase of mosfet costs for a 84 V configuration is shown in Fig. 6. On the other hand, at a given output voltage, the costs of the mosfets, their drivers and the current sensors increase proportionally to the number of arms whereas the decrease of single inductor cost is counterbalanced by the higher number of inductors. Only the capacitor costs truly decrease when the number of arms is set at six, but this represents a very small portion of the total cost, as indicated in Fig. 6. Overall, Fig. 6 shows that the total cost is dominated by the inductor cost, up to 60 %, followed by the costs of current sensors, mosfets and their associated drivers. It has to be noted here that most cases have opted for PCB as heatsink, therefore no costs are associated with heatsinks. This is highly linked to the value of switching frequency taken for this design (i.e. 50 kHz).

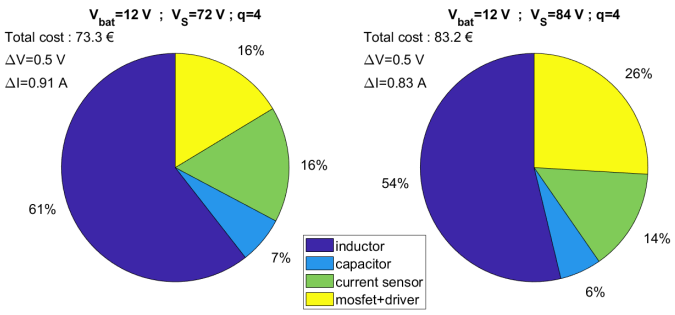

FIG. 6. Cost breakdown for two (V_S, q) configurations.

Based on results from Table 2, the configuration 72 V, four arms, is selected. Indeed, 72 V configuration is preferred over 60 V as it enables to reduce ohmic losses on the microgrid DC bus due to a lower current. Then, the four arm configuration is slightly less expensive than the three arm configuration, at 72 V. In addition, with three boost arms, to enable power modularity, only the option of having three power levels is possible. However, as the power cards are hosted on a command card, three power levels imply three power cards possibly mounted in a mezzanine-connection style and the cost of PCB to PCB connectors is sufficiently large to aim at reducing this number of connectors. Therefore, a modularity of two power levels, i.e. N_P in Table 1, is opted, which is not possible to realize with three boost arms.
Then, the costs and consequences of using one, two or four buck arms are shown in Table 3. One or two buck arms are close in terms of price, but having two buck arms enables to avoid the use of an external heatsink and to associate one buck to each power card, a feature not possible with only one buck arm. This increases the modularity of the proposed design. Indeed, if only used at half power, with one power card, only one buck arm would be mounted on the interconnection module, reducing the overall cost. In addition, the high-side buck mosfet needed in the one buck arm case is definitely more difficult to find on the market (fewer parts have all the needed characteristics), a great disadvantage due to the ongoing and unpredictable component shortage. Note here that the buck arms can not use bootstrap drivers as during normal operation the high-side mosfet is always closed. Therefore, the buck driver circuit is composed of an isolated supply, an opto-driver (for the high-side mosfet) and a low-side driver. Its total cost is set at 9 €.
This result also confirms the choice of four boost arms instead of three. Indeed, with three boost arms, the interconnection module could only contain one or three buck arms.

TABLE 3. Costs and advantages depending on the number of buck arms.

Number of buck arms N_B	1	2	4
Costs (€)	24.4	22.2	33.4
Need of a heatsink	Yes	No	No
Modularity	No	Yes	Yes
Availability of mosfets	+	+++	+++

4. HARDWARE REALIZATION

Following the previous Section results, a 30 A bidirectional buck-boost converter, composed of two 15 A power cards, each comprised of two 7.5 A boost arms and one 15 A buck arm, must be designed. In line with its particular application, the interconnection module must be straightforward to assemble and to use. Therefore, the interconnection module is composed of a command card, controlling two power cards mounted in a mezzanine-connection style. In addition, a 3D-printed casing specifically designed to enhance the user-friendliness of the interconnection module is developed.
The top layer of the command card is shown in Fig. 7, where most of its features are represented. The bottom layer contains mainly the PCB to PCB connectors hosting the power cards.
The micro-controller chosen for this design (STM32G474RE) must be at the same time able to pilot all the mosfets of the power cards at the required switching frequency and all the different peripherals on the command card (LCD screen, the RS 232 connection, etc.). It should also be able to compute in a time-efficient manner the decentralized and communication-free algorithm presented in [7].
Regarding the power supplies, to guarantee modularity of usage as indicated in the converter specifications in Table 1, a cascaded structure is adopted. A first power supply generates 15 V either from the microgrid DC bus (i.e. with a power supply input voltage around 72 V) or from the nanogrid battery (i.e. with a power supply input voltage around 12 or 24 V). Because both input voltage ranges do not overlap and are even quite different, two separate components are considered. If the interconnection module is to link a nanogrid with a battery to the microgrid, one component is used and the other footprint is not populated and vice versa. This can be seen in the lower right of Fig. 7, where two footprints are not populated : they are the ones for the power supply outputting 15 V. This 15 V power supply then is the input to the 5 V power supply. Therefore, there is only one component to change between the two proposed usages.
Finally, the film capacitors, in blue in the upper middle of Fig. 7, are the switching cell output capacitors (i.e. C_S). They are placed on the command card so that they can always benefit to both power cards. Indeed, if placed on the power cards, if only one power card were mounted (e.g. for a low power nanogrid),

the mounted power card would only benefit from half of the film capacitors. If placed on the command card, at the closest of the power card output, a good compromise between reduction of overvoltage and mutualization of film capacitors is attained. Similarly, input and output additional components are placed on the command card to further filter the input and output current and voltage respectively with C_{bat} and L_F and offer higher level of voltage inertia with a few mF of electrolytic capacitors C_F in case of large changes of operating points on the microgrid.

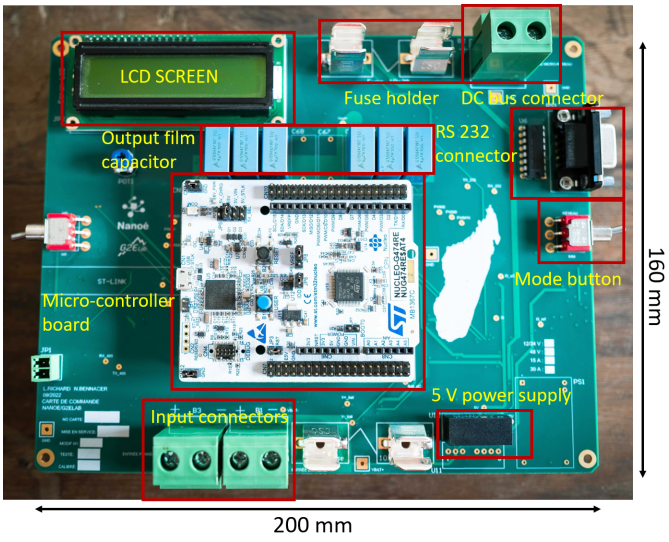

FIG. 7. Prototype of the command card of the interconnection module.

Each power card contains six mosfets for one buck arm and two boost arms, their associated command components, two power inductors, two current sensors (one for each boost arm) and some ceramic capacitors at the closest of the switching cells to reduce overvoltage at the switching of the boost mosfets. Based on results from the exhaustive search algorithm, no external heatsinks are needed and PCB as heatsink is used in the proposed design through large copper pads around the mosfets. The power card, with its legend, is shown in Fig. 8. All SMD components are located on the bottom layer (not shown in Fig. 8) whereas through-hole components (i.e. the mosfets and the power inductors) are located on the top layer. 4-layer PCBs are used for the power cards.

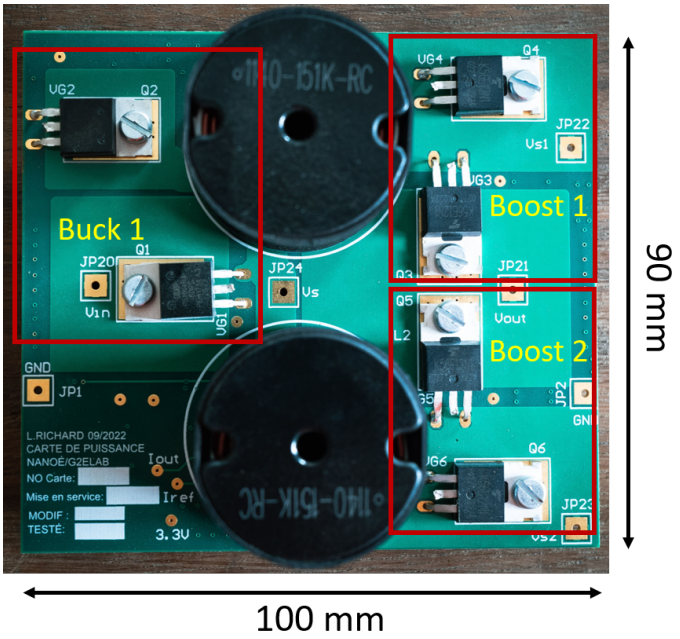

FIG. 8. Prototype of the power card of the interconnection module.

5. CONCLUSION

This paper presents the specifications and design of an interleaved buck-boost DC-DC converter used as the main brick of a DC microgrid with decentralized storage and production. An exhaustive search algorithm is proposed to cost-optimize its number of arms and the DC bus voltage, before illustrating the hardware realization of the converter.
An experimental study carried out in the lab, partially presented in [9], has then enabled to validate the proper operation of the proposed interconnection module. In particular, this converter allows for start-up and protection services, while offering a satisfying enough efficiency (above 95 % for the majority of the power range) and DC output voltage with low harmonic content. Then, 26 interconnection modules have been successfully deployed on the field in the North of Madagascar at the end of 2022 to interconnect 24 nanogrids, one nanogrid without battery and one communal load (a 750 W 48 V DC electric mill) within a village-wide microgrid [3]. As of mid 2023, the microgrid is operating well, showing the proper design of the DC-DC converter presented in this paper.
However, additional works are needed to further complete the proposed design method, with better cost modelling and inclusion of the input and output filters as well as the buck part within the exhaustive search algorithm. In addition, the switching frequency, an essential criteria of any power electronic design, should be let as an optimisation variable, after precise and thorough modelling of all its implications (losses, EMC, converter control, etc.). This will be the subject of future research.

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