HEMT GaN Normally Off Reliability comparison

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ABSTRACT - Recently, new HEMT GaN Normally Off with a buried P-layer have been developed by the LAAS Laboratory to propose a device adapted to embedded power electronics. In this article, several Normally Off HEMT GaN architectures are compared using TCAD Sentaurus simulation: Gate Recess, P-GaN, and Buried P-GaN. Main failure mechanisms are simulated and the result are compared to determine the more promising in terms of robustness for several application. The new structure with P-GaN Buried shows promising properties but needs more development to reach the PGaN and the Recess HEMT performances .

Keywords— HEMT GaN Normally Off, failure mechanism, TCAD Sentaurus, Vth stability, Gate-lag, Buffer trap, Temperature impact

1. INTRODUCTION

GaN transistors on the market are typically HEMT devices. This Normally On structure presents a heterostructure with an efficient electron path called 2DEG at the AlGaN/GaN interface. This device is currently used for RF application and is widely use because of high performances [1]: a fast switching frequency, with low losses in commutation and in conduction, and high robustness against radiation or temperature variation. In power electronics, however, a Normally Off device is required. Several studies have therefore been defined to obtain the best Normally Off HEMT GaN device, without using a solution such as another Si-transistor in cascode. While this ubiquitous solution is convenient, it maintains the Si limitation, thus the HEMT GaN development.
This article presents three different Normally Off HEMT GaN: Two topologies are developing thanks to their current possible realization for power electronic devices in harsh environment and one was recently proposed for future devices design.
In this article, after the device design description in addition of the failures mechanism presentation, we will focus on the simulation result with comparison of standard characterization. An approach on main failure mechanisms electrical behavior such as gate leakage, temperature effect, or gate degradation will also be presented. Reliability issues are indeed fundamental to the development of new power electronic devices. The simulation results will make reference to previous work comparing physically with measurements the reliability of the Recess and the PGaN devices.

2. PRESENTATION OF THE STUDIED DEVICES: SEVERAL HEMT NORMALLY OFF

We will focus on three devices: one Recess gate device[2], one commonly used P-GaN HEMT, called E-mode [3], and one Buried P-GaN HEMT [4], such as a new device in development [5].

2.1. Gate recess structure and thin barrier layer

The Recess gate HEMT (MISHEMT) bring the gate Schottky contact closer to the 2DEG channel (Figure 1) [6]. The goal is to naturally block the current in the channel with the depletion region below the gate metallization. This region become thinner as soon as a polarization is applied and the DEG current can go through. The current flow will then be pinched off at the zero gate voltage.

The Recess HEMT (MISHEMT) is look forward because of its promises for high power and present low delay for evacuating the positive carriers from the DEG channel. The Recess shows a wide interest for designers owing to its excellent gate reliability and safety. Although the Coss is a bit larger, the rise time and falling time may be reduced [7]. The consequence is a larger benefit for GaN devices in commutation.

The main drawback of this technology is the drain current reduction [8] and the high cost for obtaining a surface roughness compatible with the design conception [9]. Another difficulty is the gate recess process, not totally efficient, inducing result disparities.

In our simulation the structure keeps the same parameters as the normally-on structure but the distance d from the channel to the Schottky contact will be adapted to obtain the desired result (Figure 2).

With Recess Gate structure, the AlGaN barrier is etched. It unfortunately often creates many defects in the barrier layer, damages density and mobility of 2DEG [4]. To avoid etched barrier, P-GaN and buried P-GaN structure were developed.

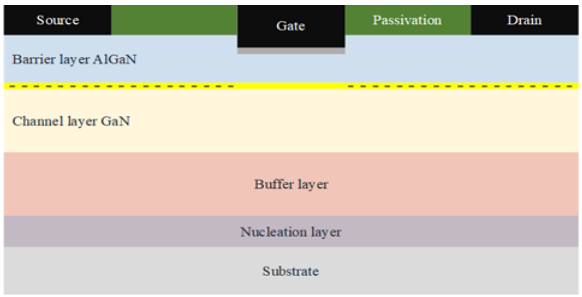

Figure 1: Recess Gate technology

2.2. P-GaN Gate HEMT

In this structure, a GaN layer doped P with Silicon doping is introduced below the gate contact region and over the 2DEG (Figure 3). The P-GaN layer lifts up the band diagram, resulting in the depletion of the 2DEG channel (Figure 4), even without external applied bias (V_G = 0). The consequence is the possibility of easily modifying the threshold voltage, setting the P doping concentration. This technology is, albeit, rather challenging to realize, and the device electrical behaviour is significantly influenced by several layouts and processing conditions [3] limiting the device reproducibility.

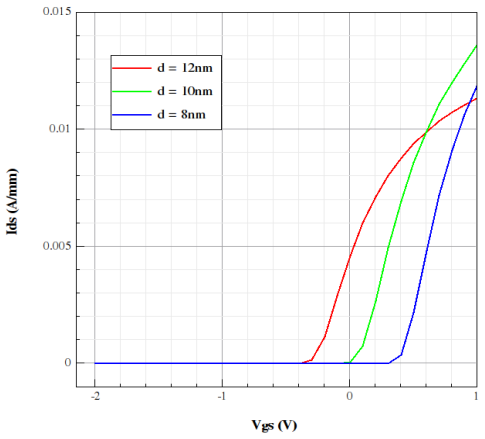

Figure 2. Vg-Id characteristic with different distance d of Recess Gate HEMT normally-off, under Vds = 0.1V.

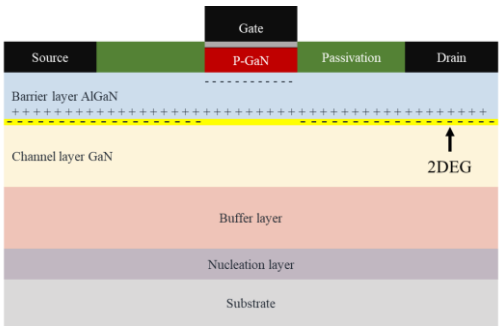

Figure 3: E-HEMT GaN Technology

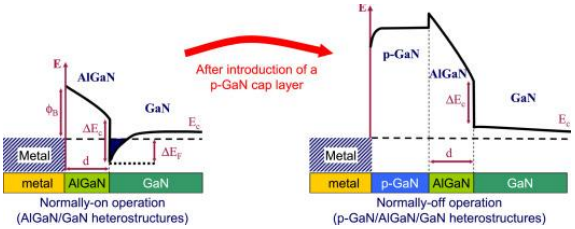

Figure 4. Band diagram of HEMT GaN before and after inserting p-GaN layer [11]

The P-Gan doping concentration was optimized for obtaining the highest threshold voltage and was fixed at 5e18 p/cm^{-3} with magnesium atoms.

2.3. Buried P-region

The cross-sectional structure of this new HEMT Normally-Off is shown in Figure 5. A P-GaN layer, doped with Si, is inserted below instead of above the 2DEG as in the precedent device. If the doping concentration is high enough, the conduction bands will be sufficiently elevated, beyond the Fermi level. As a result, the 2DEG channel will be deserted and the HEMT will become Normally-Off. A positive voltage has then to be applied to the gate for carrier conduction in the DEG. Furthermore, the N-GaN regions should be implanted below the 2DEG to restore the channel regardless of the gate voltage value [3]. As described in the figure, the P-doping is localized at gate level.

At the beginning, the positive bound charge at the interface AlGaN/GaN push the 2DEG triangle well downwards, below the Fermi level. To achieve the normally-off operation, the P-GaN region has to be enough effective to uplift the conduction band in the vicinity of the AlGaN/GaN interface or the positive bound charge has to decreased followed by the downward shift of the 2DEG level. With the first option, P-GaN region depends on the thickness and the concentration and its effect is not sufficient to uplift the triangle well sufficiently. The second option is then recommended. The x mole fraction in AlGaN barrier layer should be decreased in order to reduce the AlGaN layer strain. As a result, the piezoelectric polarization and the bound charge are reduced. A trade-off has to be optimized with Ids hence the two options are combined to create a normally-off structure with enough current.

The idea of buried P-GaN region is promising but its fabrication is really a big challenge and presents two options. The first option is the ion implantation but doping concentration will be relatively low. The second one is localized epitaxial growth but is really challenged and expensive [1].

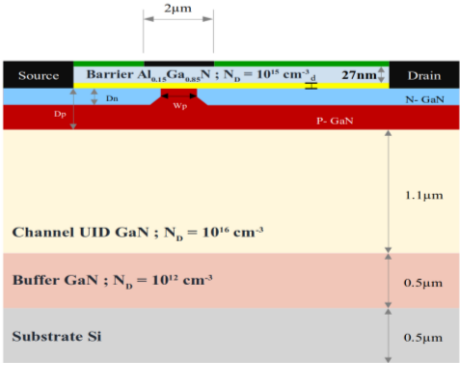

Figure 5: Cross-section structure of Buried p-region HEMT

The first experimental demonstration of this new structure was presented in [5] in 2018. It concludes that the appearance of the P-GaN layer (doping about 2x1018cm-3) allows the conventional HEMT to shift the threshold voltage from -5.5V to 0.8V.

Based on the simulation results of previous research, the following (Table 1) parameters will be applied for simulation.

Table 1: Parameters for simulating Buried p-GaN region structure.

Passivation thickness	dins	10nm
AlGaN barrier thickness	tAlGaN	27nm
x mole fraction	xAlGaN	0.15
Distance from interface AlGaN/GaN to P-GaN region	d	From 10nm to 30nm
P-GaN thickness	Dp	100nm
P-GaN width	Wp	1µm
P-GaN concentration	Np	From 5e^{17} cm^{-3} to 3e^{19} cm^{-3} (doping Magnesium but in Sentaurus, Boron was used)

The following results (Figure 6) illustrate that Buried P-GaN region structure gets the normally-off operation. The N-GaN regions are doped Silicon (but in Sentaurus, Arsenic was used) 10^{18} cm^{-3}, and size 40nm of thickness.

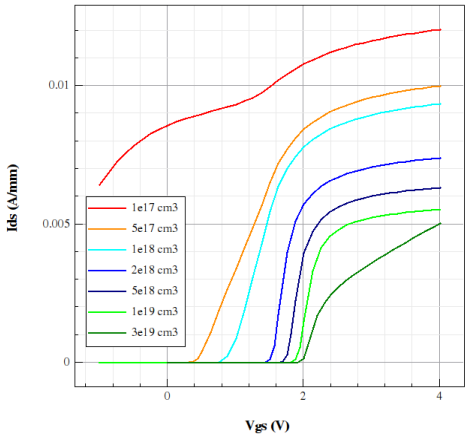

Figure 6. Vg-Id characteristics with different Np of new Buried P-GaN structure, at d = 10nm, under Vds = 0.1V.

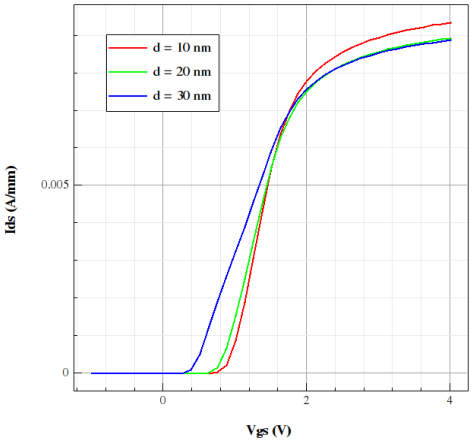

Figure 7. Vg-Id characteristics with different d of new Buried P-GaN structure, at Np = 1e18 cm^{-3}, under Vds = 0.1V.

3. FAILURE IDENTIFICATION

This part will explain what are the main failures related to GaN technology transistors. This analyse is not exhaustive but summarizes the frequent undesirable effect. We will therefore try to simulate some of them in order to observe their electrical signature and to compare which technology seems more robust.

The HEMT GaN failures are classified into parasitic and dispersion effects and reliability issues [10]. The simulation will not be carried out on the first because progress has to be realized directly on the material quality, independently of the device architecture and the simulation result will not be coherent with this atomic and hazardous topic.

The Figure 8 presents the popular degradations in HEMT GaN [2]. The red region refers to the failures due to thermal stress, while the blue regions focuses on failures caused by hot-electrons and while the green region are related to GaN material with spontaneous and piezoelectric polarization effects. The following explanations will present how these failures proceed and we will comment on their possible simulation with TCAD Sentaurus.

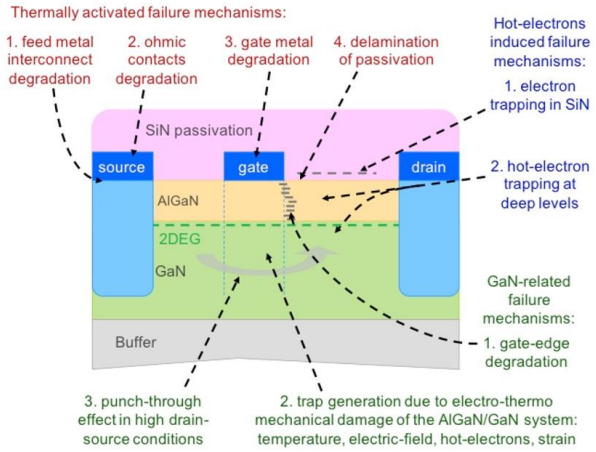

Figure 8. Illustration of the main degradation mechanisms in GaN HEMT [5]

3.1. Contact degradation

In HEMT AlGaN/GaN Normally On, the gate Schottky contact gate is often made of Pt/Au and the drain and source contact made of Ti/Al/Pt/Au [11]. Under thermal stress, the two main degradation mechanisms are Au inter-diffusion inside the metal layers and Ga out-diffusion from semiconductor into metallic compounds [11]. The contact reliability depends on the fabrication process and on the metal settings. These conditions should be optimized to reduce the poor performance due to contacts degradation.

In our simulation, we will not simulate an alloy degradation of the gate, neither a particle diffusion. We will only modify the gate length to observe its impact. Drain and Source contact length degradation are not simulated because this contact is made usually stronger than those of Gate contact.

3.2. Temperature effect

In semi-conductor physic, the temperature is a critical parameter and often generates degradations. As we can see in red on the Figure 9, several issues are depending on the temperature. For example, the decreases in $R_{DS(ON)}$, the decrease in I_{DS}, or a Vth negative shift are observed with the temperature increase for p-GaN HEMT [12]. These result physically observed and it will permit to calibrate our simulation and verify the result accuracy.

3.3. Hot-electrons induced

In general, 'hot electrons' are electrons attaining very high kinetic energy due to very high electric field. These high-energy electrons can be injected into and trapped in the regions of transistor HEMT GaN like surface of passivation, barrier AlGaN or GaN buffer layer, leading to transconductance degradation and can saturate the drain current [11]. Passivation electrons trapping is described as follow: at high bias voltage to the gate, some electrons are tunnelling from the gate to the surface passivation/AlGaN while a large amount of current is generated by drain polarization in the 2DEG. These electrons achieve very high energy and become hot electrons: they move freely in the structure, collide with crystal lattice and get easily trapped in the GaN buffer layer, or depending on the kinetic energy, in the AlGaN barrier [12]. This phenomenon depletes partially the 2DEG channel and degrades the drain current in the channel. As a consequence, the pinch-off voltage is shifted, the on-resistance increases and the transconductance is reduced. A solution to inherently prevent this kind of problem in bipolar transistor is to reduce the P doping in the basis [13]. The PGaN device should hence present the worst due to its structure with high electric field on P doping. A solution is to add a resistance on the gate control but it will also add some electrical losses. The Buried and

the Recess might be more performing for high electric field application such as for 1200V devices.

No simulations are dedicated to this problematic because this study can be only experimental. Indeed, as soon as hot electrons appears after aging, the device is considered as broken whereas hot electrons are initially considered in simulations. There is therefore no interest to study their apparition in the device.

3.4. GaN-related

A. Gate-edge degradation

This degradation appears when high reverse bias voltage is applied to the gate: at the electrode's edge, where the electric field is the highest, electrons are injected from the gate to the AlGaN due to the inverse polarization effect [7]. It results a mismatch between AlGaN and GaN's crystal structure. Thereby, if the elastic energy at AlGaN/GaN layer surpasses a critical value, crystallographic defects will be formed, degrading the device performances.

Some additional traps are injected at AlGaN/GaN interface, but the result is similar for the three structures and will hence not be presented. Otherwise, the leakage current was observed during reverse polarisation on the gate.

B. Punch-through effect

When high drain voltage overwhelms the nominal voltage, the electron current flows through the deeper layer such as GaN layer. This mechanism can be reduced by changing the doping density in the buffer layer or in adopting a double hetero-structure configuration [12].

Static simulations will be carried on until the avalanche voltage to evaluate the intrinsic reliability of each topology in Off and in On state. Even if some parameters are adjustable during the processing for increasing the avalanche voltage, the simulation will give us the best adapted topology for high voltage application.

4. SIMULATION RESULTS

First of all, TCAD Sentaurus is used to construct the conventional HEMT, the dimension and doping concentrations parameters are showed in Table 1. For all devices, the same geometry is respected with a gate larger equal to 2µm, a distance from source to gate equal to 2µm and a gate to drain equal to 5µm. Si_3N_4 is selected for passivation layer. The thickness of this layer is adaptable in order to current-collapse elimination requirement. AlGaN and GaN are doped type-n with Arsenic in Sentaurus model, even if others impurities may have been used [14]. Source and Drain contacts are Ohmic contacts, with a type-n implantation, while gate contact is a Schottky contact. In all cases, the work function parameter is fixed similarly at 5,1eV. In AlGaN barrier layer, the thickness and x-mole fraction (% mole of Al in AlGaN) are extremely important since they are used to define the Sheet Charge at the AlGaN/GaN interface. 30nm and 0.25 are respectively the values of the original structure. Using the HeteroInterface and Piezoelectric Polarization (strain) as Physics models, Sentaurus calculates automatically and creates this 2DEG channel. An extremely thin *Delta* layer was created at the interface AlGaN/GaN with a value of Sheet Charge equal to the peak doping which is calculated by piezoelectric and spontaneous polarizations between both materials. Theoretically, the Sheet Charge is calculated at 8.45e12 cm^{-3} thanks to the following parameters: A 10nm layer of UID GaN channel, doped at 10^{16} cm^{-3} is created to ensure a dense enough meshing at the interface. For the meshing, a trade-off between the convergence and the simulation time has to be found. The calculation cannot converge if the step size in *Solver* and if the size elements in the meshing are not reasonably adjusted, mostly in the sensitive regions such as the electrical interfaces. In the conventional HEMT model of Sentaurus, the interface region AlGaN/GaN and under-gate regions are the most important ones. The device is meshed with around 20000 points and the minimum sizes (x_{min} and y_{min}) of the mesh elements for sensitive regions can locally decrease to 0.01nm.

All DC stress simulations (Vg-Id and Vd-Id) use the same material parameters, the same physical model and the same temperature condition. The meshing method and the density of AlGaN/GaN interface bound charge will be slightly adapted to each structure. Note that for all result, the ylegend indicates the current [A] but the simulation are still run in 2D, meaning, the ylegend should be the density current in [A/mm].

The simulation results will be compared between the experimental result known in literature for Recess and PGaN [15] [16]. Hypotheses deduced on these simulations will mainly be in concern with the Buried PGaN device.

4.1. Static characterization

4.1.1. Id-Vg

First we simulate the drain current versus the gate voltage for the three devices (Figure 9).

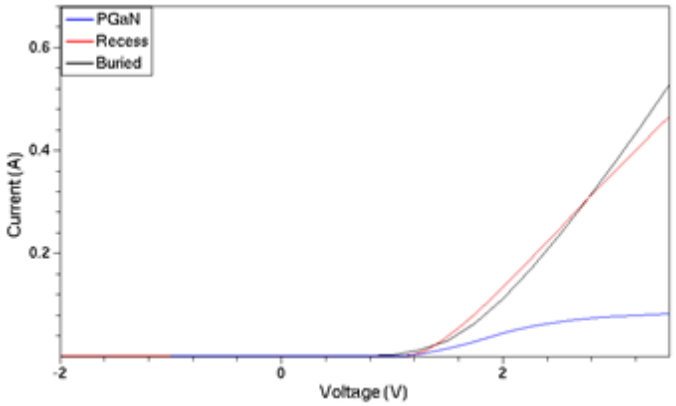

Figure 9: IdVg simulation for Recess HEMT, PGaN HEMT and Buried PGaN HEMT

The Recess threshold voltage is usually lower in comparison with the others devices. Although a trade-off between AlGaN width layer and the threshold voltage was found, a higher V_{th} value can't be obtained with this topology. As indicated in [15], a common Vth value is around 1.5V. In this work, we set the threshold voltage at around 1.3V for all devices.

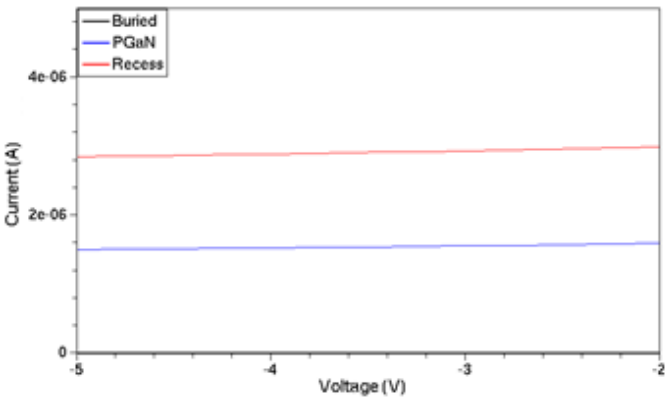

Figure 10: Leakage IdVg Simulation for Recess, PGaN and Buried HEMT

For the other topologies, the Vth value is depending of the PGaN doping concentration. Indeed, increasing the doping concentration below the gate electrode is easier for obtaining a Normally Off state device. P doping area dimensions are adjustable in addition to the doping concentration. Although obtaining a high P doping is laborious, a maximum threshold voltage value is rapidly reached near 4V. In case of the Buried,

the AlGaN layer can also be adjusted. This device present therefore more flexibility.

Concerning the leakage drain current in Off state, from -5V to 0V, the Buried device presents the best performances (Figure 10). The Recess device has logically the worst performances because the current can easily go through the channel than in other case where electrons are mainly recombined by the holes.

4.1.2. Id-Vd

The second standard characterization is the drain current versus the drain voltage. The simulation is carried out until Vds=600V (Figure 11) and until failure (Figure 12) for Vgs=0V and Vgs=4V. For each case, the transistors are logically Off at 0V even if a leakage current is observed on P-GaN and Recess devices, as it is shown in Figure 13. The current increase until around 0.3 mA, which creates some energetic losses in Off state. The P-GaN is less efficient than the Buried HEMT whereas it was expected for the recess device.

In Figure 11, we can observe the good performances of the three devices until 600V, the most common application for HEMT GaN normally off devices, with a current level not totally fixed for the three devices. Several physical parameters and doping can be adjusted to obtain an identical current.

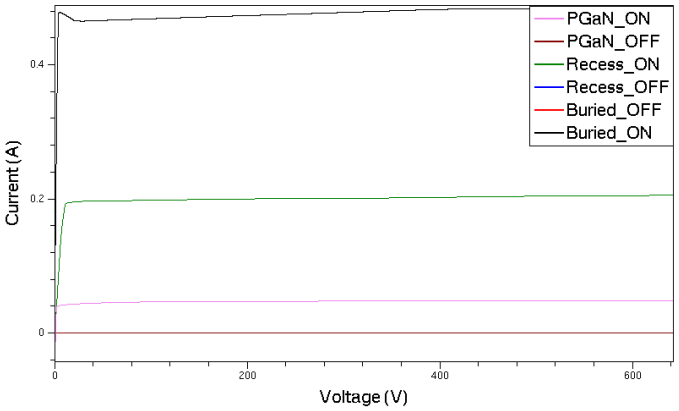

Figure 11: IdVd result simulation for Recess, PGaN and Buried HEMT in On and Off state until 600V

Buried GaN device and PGaN should logically display a higher robustness to the punch through effect than Recess device because of its larger AlGaN layer. The maximum voltage is yet to be determined to guarantee a robust utilization.

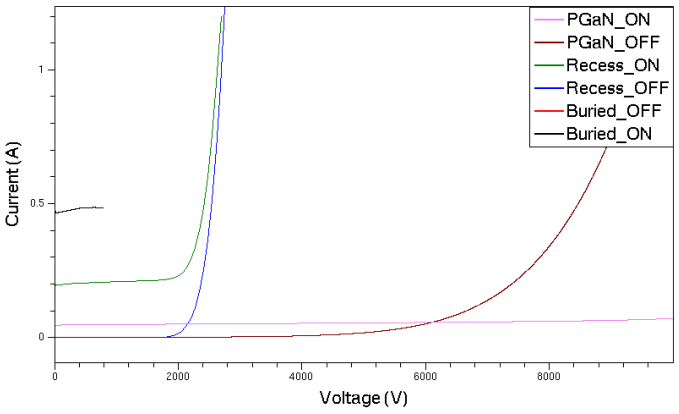

Figure 12: IdVd simulation for Recess, PGaN and Buried PGaN HEMT

In Figure 12 however, the P-GaN presents largely the best performances with a current increase in OFF mode due to avalanche after 4kV. Then the Recess device presents a similar behaviour at around 2kV. The Buried device unfortunately didn't converge after 800V, limiting the interpretation results.

When Vgs=4V, hence when the device is in ON mode, the electrical behaviour is identical. They all conduct until more than 800V, before the simulation stopped for the buried device and before avalanche for the Recess device. The PGaN device looks really robust however, the technology to obtain higher electric field.

The internal resistance noticed are logically similar for PGaN and Buried at respectively around 12Ω and 10Ω instead of 13Ω in[16] whereas for Recess the resistance is estimated at 55Ω instead of 22Ω.

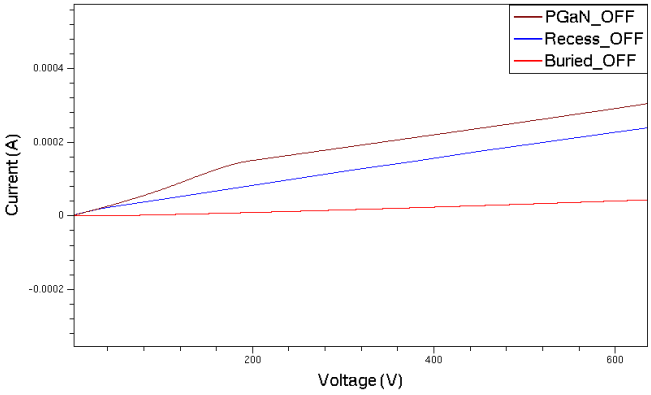

Figure 13: IdVd result simulation fo Recess, PGaN and Buried HEMT in Off state until 600V

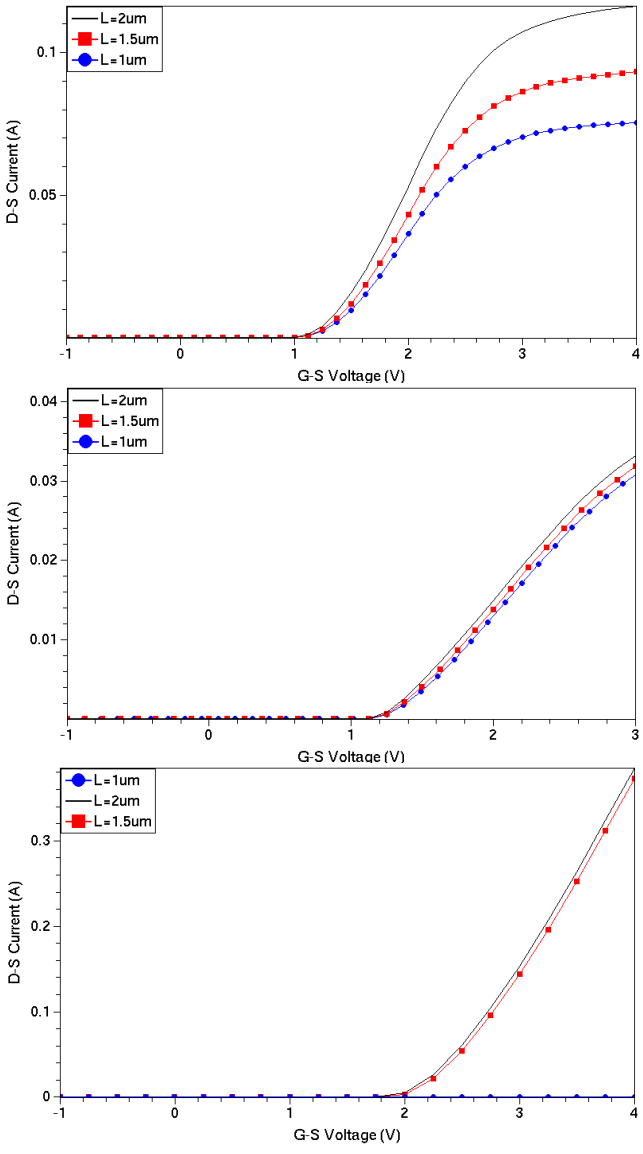

Figure 14: IdVg simulation for several gate length for respectely: Recess, PGaN and Buried HEMT

4.2. *Contact degradation results*

The contact degradation is simulated in Figure 14. This failure mechanism is modelled by the gate size reduction. Therefore several gate size have been evaluated and the electrical impact seems minimal on the Recess and on the PGaN devices. Indeed, even with a 25% width variation, the threshold voltage stay identical. In [15], the gate length had a strong impact on Ron for Recess device. Finally the Buried GaN seems the less sensible but its current fall down when the gate length becomes too short. The PGaN device looks more stable than the Recess configuration device with less Ron variation. This behaviour appears coherent with [15] where they present the PGaN as the more accomplished device, until at least 600V. Physically, there is few differences with the Buried whereas the Recess is more sensitive with dielectric traps carrier or dielectric breakdown.

4.3. *Temperature variation robustness*

The ambient temperature is modified in this part to evaluate the electrical behaviour on IdVg (Figure 15) when the temperature varies from 270°K to 410°K, corresponding respectively to -3°C until 130°C. These values are common temperature variation in power electronics and results in term of electrical behaviour can be surprising with strong variations.

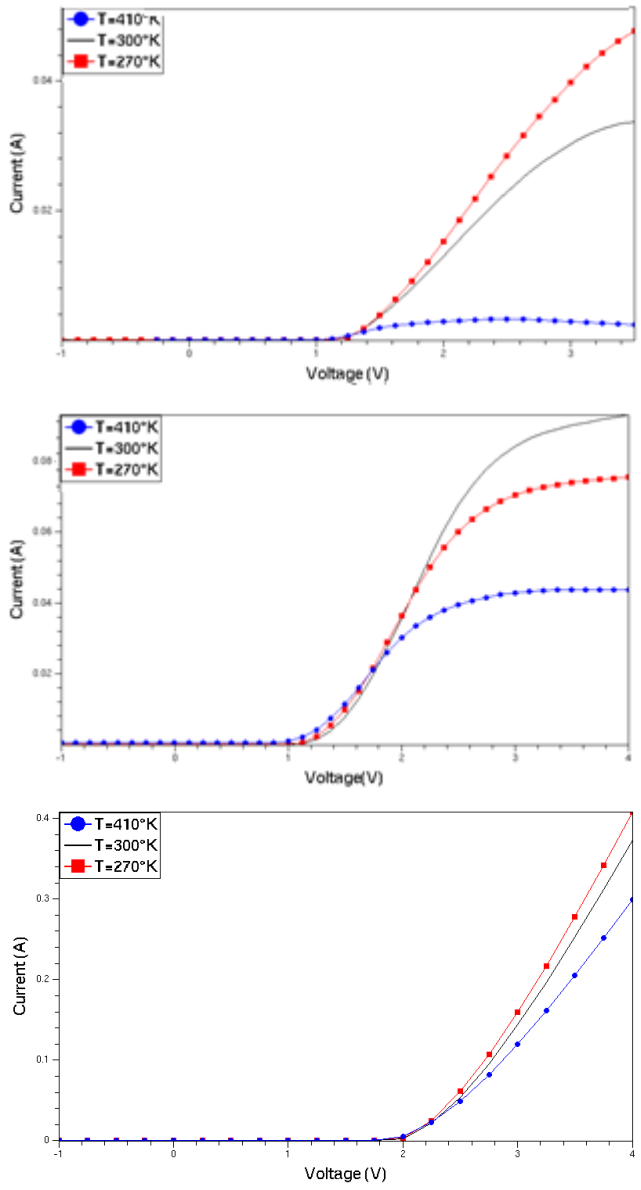

Figure 15: IdVg simulation for several temperature for respectively: Recess, PGaN and Buried HEMT

The Buried device look very robust in comparison with others. Only few variation are observed whereas for PGaN and Recess an additional current is observed at 270°K with a reduction at 410°K. The Recess is more strongly impacted by the temperature variation and the current observation for T=410°K let us sceptical for power electronic application. As the length variation, the Ron impact for the Recess is fundamental.
A technical solution is proposed in [17] during the device realization process: It is suggested to use GaN HEMT transistors with hydrogen plasma treatment instead of etching technology to reduce leakage current and increase threshold voltage stability.

5. CONCLUSIONS

Two main architectures of Normally Off HEMT GaN devices are compared by simulation to a new device in this article. The realization process aside, the Buried PGaN below the 2DEG device seems more reliable than the PGaN for high power application because of its high gate robustness, its better electrical behavior, and because of its probable hot electrons robustness capacity. This structure is a serious concurrent to the Recess device for high voltage application with a better theoretical Ron stability.
Even if the P-Gan HEMT is the current solution used by industrials in addition of the cascode device for 600V application, the solution presented is less sensitive to temperature variation, with less leakage current, and less impact of the gate degradation. Furthermore, the threshold voltage setting is much easier to fix and can facilitate the adequate driver.
Such device can be really precious to create an unique architecture for the whole voltage range of Normally Off HEMT GaN devices, even if fabrication processes are not taken into account,

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