A study on the challenges in GaN HEMT-based designs from component to board development level

Thilini Wickramasinghe[1], Bruno Allard[1], Christian Martin[1], René Escoffier[2]
[1]Univ Lyon, INSA Lyon, Université Claude Bernard Lyon 1, Ecole Centrale de Lyon, CNRS, Ampére UMR5005, F-69621 Villeurbanne, France. [2]Département DCOS, Laboratoire LC2E, CEA-Leti, Grenoble, France.

***Abstract*—A study on a few main challenges in GaN-based designs from component to board development level is presented. The circuits of GaN transistors in parallel in a high-speed switch are more critical for power converter designers as they are sensitive to parasitic components in both power and gate control circuits. Besides, the effect in switching behaviour caused by the device parameter discrepancies are yet to be realized. In this study, both experimental and simulation-based approaches were used for the verification of board parasitics and parametric discrepancy effects. A Spice simulation model combined with experimental data was used to estimate the effect due to parametric variation of devices in parallel.**

***Index Terms*—GaN HEMTs, paralleling, parasitics, non-identical components, high speed switching**

I. Introduction

The Gallium Nitride (GaN) based high electron mobility transistors (HEMTs) are capable of applying in high switching frequencies (over 200 kHz) which, can improve the power density and efficiency of converters. However, high frequencies above the 100 kHz significantly increase the vulnerability to frequency dependent parasitic elements in both the power and the gate control circuits. Due to those parasitic elements, unpredictable high current and voltage spikes can be generated during switching transitions.

GaN HEMTs have (i) rigorously limited gate voltage ranges (very low safe margins) with high electron mobility, and (ii) low threshold voltages. Therefore, they are very sensitive to fast voltage and current transients which cause spurious turn-on or ultimately damage the sensitive gate structure.

At preset, the GaN HEMTs are evolving very fast but the manufacturing process is not matured as the Si-base production. Therefore, the consistency of device electrical properties is often subject to change. Most GaN HEMT manufacturers are yet to confirm the reliability of their products to implement confidently in commercial applications. To guarantee reliable operations, more research on device parameters are required. Especially, the switching behaviour of many GaN devices in parallel can be affected by the variations in device electrical properties. This phenomenon has not been investigated extensively.

In this study, the board level issues and electrical property mismatch of the GaN HEMTs in parallel were investigated using three different circuit designs. The targeted applications of the transistors are low voltage converters (such as 48 to 12 V). An H-bridge switching cell was analyzed using experimental and simulation-based approaches to verify both parasitic and parametric-discrepancy effects. Two relatively matured GaN devices from GaN Systems inc were used for the analysis.

II. Board Level Issues

In [1]–[3], the circuit board level parasitic effects and their significance on the switching operations were examined. They have been found that a high impact on switching behavior is caused by (i) the stray inductance of main power loop, (ii) the mutual inductance between power and gate control loops, and (iii) the quasi-common source inductance [1]. Multi-layered circuits with symmetrical designs were proposed in [1] to reduce length of routing and therefore minimize parasitic inductance losses. However, to identify the impact of the layout and to evaluate the current distribution among transistors, single layered PCBs were sufficient [2], [3].

The ideal method to measure the current distribution among transistors in parallel is to monitor the current in each device. In GaN HEMT-based fast switches, the current waveforms have very high frequency harmonics (from tens to hundred of megahertz). Therefore, fast responding sensors with wide bandwidth are required [3], [4]. Although inline sensors can add more parasitics to the circuit, current sensing shunt resistors (current viewing resistors—CVR) found to be the best solution at present. They have an extremely flat frequency response from DC to 2 GHz. However, insertion of some low inductive, high precise CVRs on the circuit is a challenge due to their physical dimensions.

In [5], a study on CVR-based drain current measurements of four identical GaN transistors in a fast switching cell was presented. The schematic of the cell is illustrated in Fig. 1.

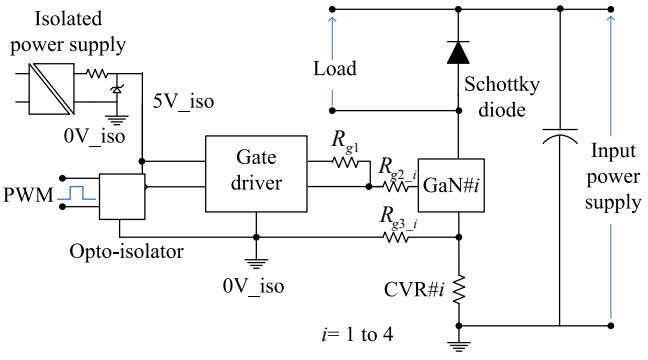
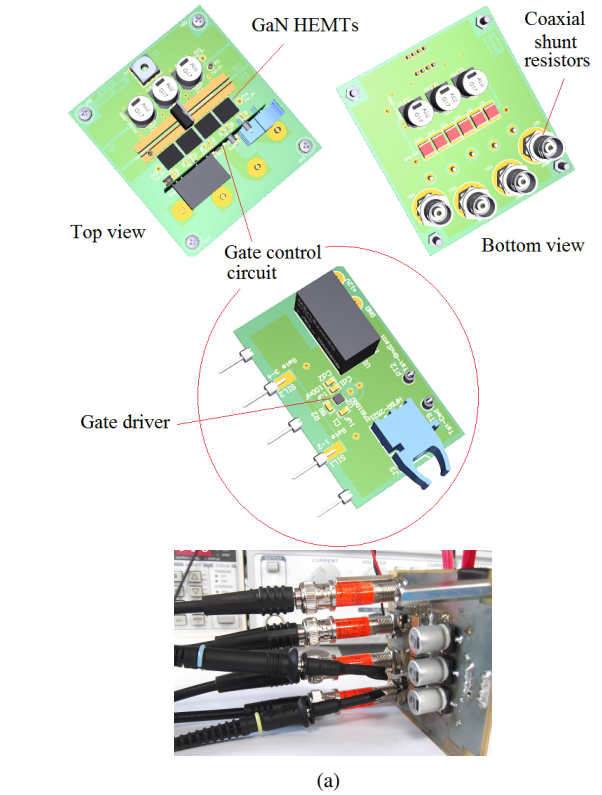


Fig. 1. Schematic diagram of the four GS66516T-based test prototype.

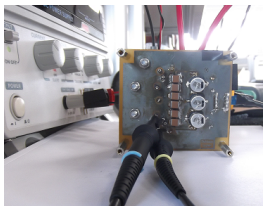
Two symmetrical layouts as summarized in Table I were built to investigate the consequences of adding CVRs in the power path. As seen in Fig. 2, four parallel devices were on the top-side of the PCB#1 while in the PCB#2, the devices were placed both sides (see Fig. 3). The CVRs used in PCB#1 were stud-type coaxial shunts and they were mounted between the ground and the source terminals of the low-side switch.

TABLE I
TEST PROTOTYPES FOR BOARD-LEVEL PARASITIC COMPONENTS (GS66516T-BASED CIRCUIT)

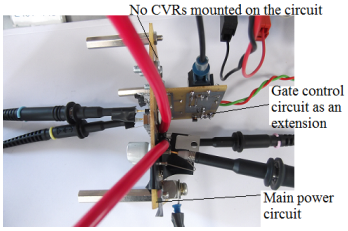
Exp#	Circuit Layout	PCB design	Identical devices	No. of parallel devices	Current sensor
1	Symmetrical	PCB#1	Yes	4	CVR
2	Symmetrical	PCB#1	Yes	4	None
3	Symmetrical	PCB#2	Yes	4	None



(a)



(b)



(c)

Fig. 2. Four GaN HEMTs in a line laid configuration (PCB#1): (a) the PCB design and the CVR mounted test prototype, (b) the board without CVRs, (c) side views of the board without CVRs and the connections of test probes.

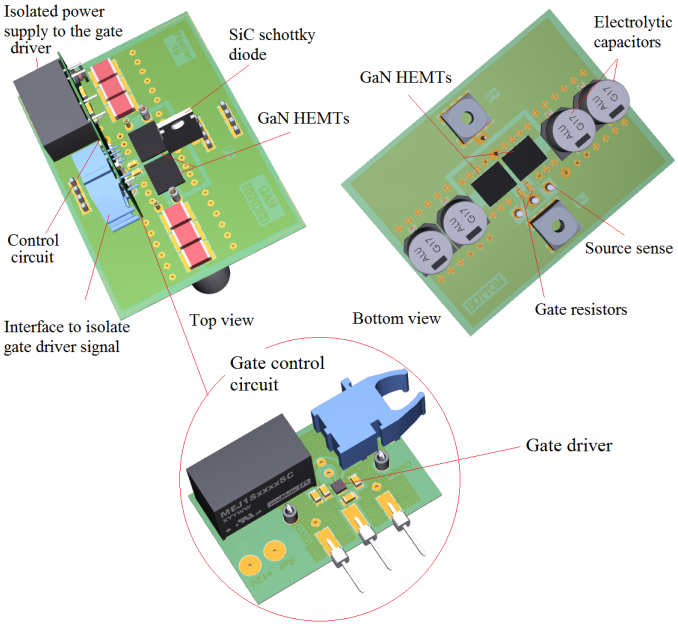


Fig. 3. The design of the PCB#2 (without CVRs): four GaN HEMTs in parallel on two sides of the board.

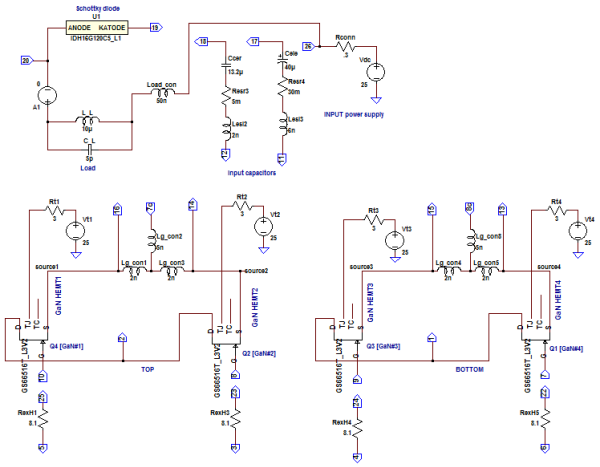


Fig. 4. Power-loop simulation model of PCB#2 with parasitic components.

The layout of GaN HEMTs on PCB#2 is more symmetrical than the PCB#1and the design eliminated the CVRs. Therefore, no physical current measurements can be obtained from the PCB#2. To estimate the current through the parallel devices, an LTSpice simulation model was built and Fig. 4 illustrates its power-loop.

In the experimental setup of the PCB#1, two oscilloscopes were used to observe the outputs of CVRs and other measurements simultaneously. The voltages across CVRs were recorded using a digital phosphor oscilloscope (Tektronix DPO4034B, 350 MHz, 2.5 GS/s) while the load current, drain and gate voltages were measured by a mixed domain oscilloscope (Tektronix MDO3024, 200 MHz, 2.5 GS/s). Further,

BNC cables for CVRs, high bandwidth passive probes for other voltages (Tektronix P6139B—500 Mhz) and a current probe for load measurements (Tektronix TCP0030A—DC to >120 MHz, 30 A—maximum range) were used.

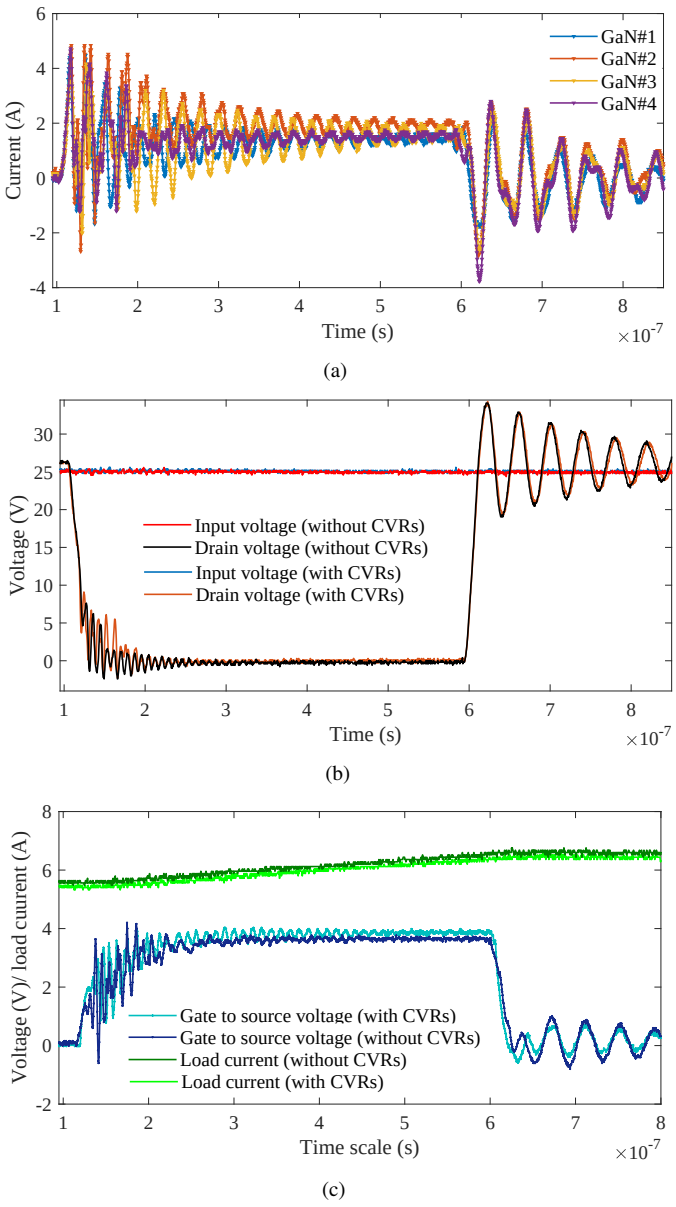


Fig. 5. The results with and without connecting CVRs: (a) CVR-based current measurements, (b) a comparison of drain and input voltages, (c) a comparison of load current and gate–source voltage [3].

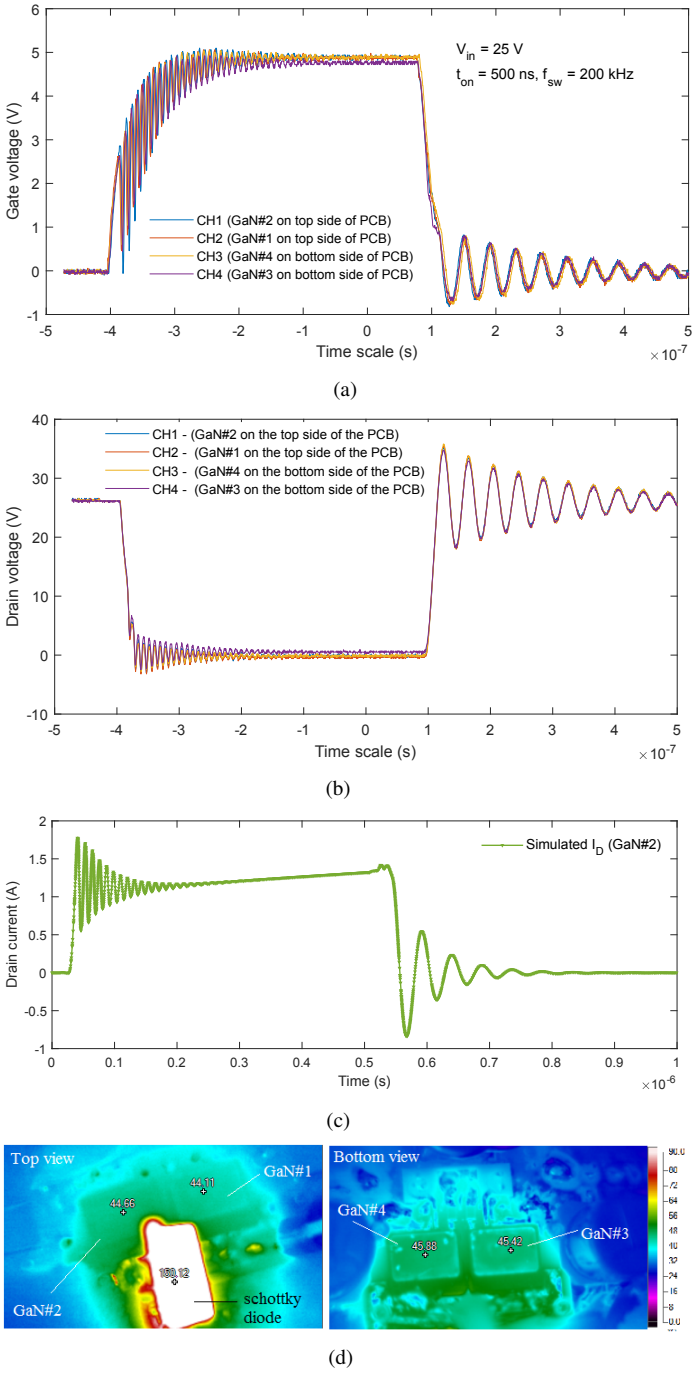


Fig. 6. PCB#2 results: (a) gate voltages of the four GaN HEMTs in parallel, (b) drain voltages the four GaN HEMTs, (c) simulated drain current through a GaN HEMT, (d) thermal images of the two sides of the PCB [3].

The CVR-based current measurements of the PCB#1 are illustrated in Fig. 5(a). Despite the high oscillations, comparably similar current distribution and a stable thermal equilibrium among the four parallel devices were observed. The drain and the gate voltages were compared with and without CVRs mounted on PCB#1 and the results are shown in Fig.s 5(b) and 5(c) respectively. Due to the insertion of CVRs, the power rails in PCB#1 had to make long which add more parasitics to the circuit and thereby more oscillations.

Figures 6(a) and 6(b) illustrate the measured gate and drain voltages of the PCB#2. When estimating current using simulation model, the manufacturer (GaN Systems inc.) provided device models included. The values of the parasitic components of the circuit model (Fig. 3) were extracted using ANSYS Q3D software. As seen in Fig. 6(c) the oscillations in current are much lower than the PCB#1. For further confirmation of uniform current distribution, the thermal images in Fig. 6(d)

were obtained.

As seen in the above experimental results, the inclusion of large current sensing resistors has negative impact on the drain voltages and current readings, and it also can modify the gate signal.

III. COMPONENT LEVEL ISSUES

The GaN HEMTs are desirable to parallel as they have a positive temperature coefficient in the on-resistance provided that the threshold voltage is relatively stable over wide temperature range. In practical situations, these electrical parameters can be varied to some extend. However, there are less studies on GaN HEMTs in this regards.

In [6], the switching behavior of two parallel Silicon Carbide (SiC) transistors with dissimilar R_{on} and threshold voltages V_{th} in parallel has been investigated. The dissimilarities in R_{on} and V_{th} of the two parallel devices were approximately 10% and 25% respectively. The experiments were conducted from 30 to 100 kHz switching range. The study showed that the R_{on} influences the static current sharing while V_{th} influences the dynamic. Further, less switching losses can be expected in devices with low gate charges and low gate resistances. Similar to [2], here the effect of utilizing inline current sensors has not been considered for the measurements. The GaN-based switches operate faster than SiC. Therefore, the impact of GaN device parameter variations (R_{on} and V_{th}) on high-speed switching can be different.

In this study, a theoretical analysis has been conducted to investigate the effect on the current distribution among two parallel GaN transistors due to the variation of these on-resistance and threshold voltage. Then, they were verified with experimental results.

A simulation model of a switching cell shown in Fig. 7 was built with commercially available GaN devices from GaN Systems Inc. (GS66508T). The device model includes the package parasitics (i.e. gate connection is 0.4 nH, source is 0.04 nH and gate is 1 nH in series with 0.72 Ω). Further, the device parameters R_{on} and V_{th} were change accordingly to vary the values of two parallel GaN HEMTs of the low-side switch. The simulation conditions are summarized in Table II.

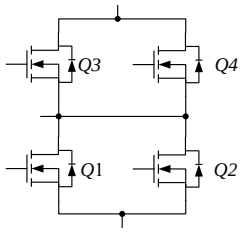


Fig. 7. Schematic diagram of the switching cell

Figure 8(a) illustrates the effect on threshold voltage variation in two parallel devices (i.e. Q1 and Q2, the dispersion of V_{th} in 1 and 10%) when the on-resistances are identical while in Fig. 8(b) vise versa. As seen in the results, the dissimilarities in on-resistance is not significant compared to the mismatches in threshold voltage simulation results. The board level parasitics were not considered for this analysis.

TABLE II
SIMULATION CONDITIONS AND RESULTS

Parameter	% (Q1 - Q2)	Low-side		High-side		δI_{ds}^{peak}(%)	
		Q1	Q2	Q3	Q4	Q1	Q2
V_{th}(V)	1%	1.313	1.3	1.3	1.3	+6.4	−5.8
(R_{on}=50mΩ)	10%	1.43	1.3	1.3	1.3	+57	−62
R_{on}(mΩ)	1%	50.5	50	50	50	+0.3	−0.5
(V_{th}=1.3 V)	25%	62.5	50	50	50	+10	−10

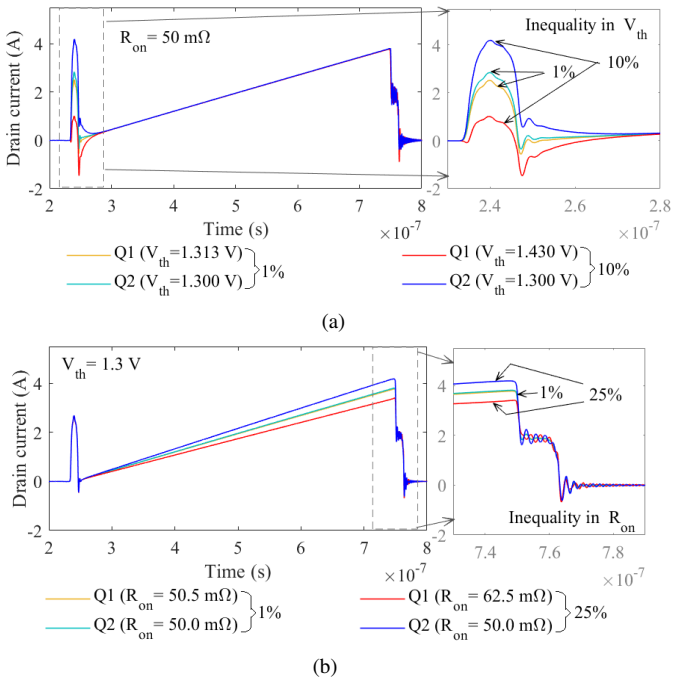


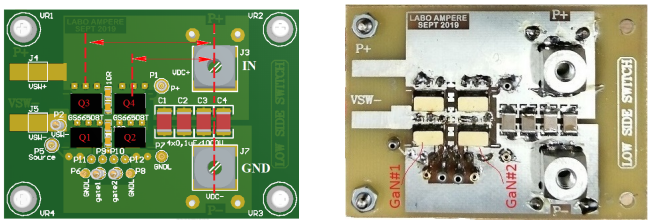
Fig. 8. Simulation results of the two parallel GaN HEMTs (GS66508T) devices with electrical property discrepancies: (a) when V_{th} varies, and (b) when R_{on} varies.

IV. EXPERIMENTAL VERIFICATION

Two experiments as summarized in Table III have been conducted to analyze the effects on board level parasitic components when the device parameter discrepancies are present. The board level parasitic effect was evaluated by comparing the results of identical parallel device in the asymmetrical circuit. To investigate the significance of device parameter mismatches when layout is unbalanced, the circuit was tested with nonidentical components.

TABLE III
TEST PROTOTYPES FOR BOARD-LEVEL PARASITIC COMPONENTS AND DEVICE PARAMETER DISCREPANCIES (GS66508T-BASED CIRCUIT)

Exp#	Circuit Layout	PCB design	Identical devices	No. of parallel devices	Current sensor
4	Asymmetrical	PCB#3	Yes	2	None
5	Asymmetrical	PCB#3	No	2	None



(a) (b)

Fig. 9. Circuit layouts for GS66508T (PCB#3) with no CVRs: (a) the PCB design, (b) the test circuit board.

Firstly, the parametric tests were performed on a set of GaN HEMTs to identify their dispersion and differentiate (i.e. identical/ nonidentical). The electrical parameters over 5% variation with the datasheet values were considered for the nonidentical component-based circuit.

The first experiment was to investigate the significance of device parameter mismatches when unbalanced layout parasitics are presented. Figure 9 shows the PCB design. In the layout, the input to the high-side drains and the ground to the low-side sources of the switching cell were unequal.

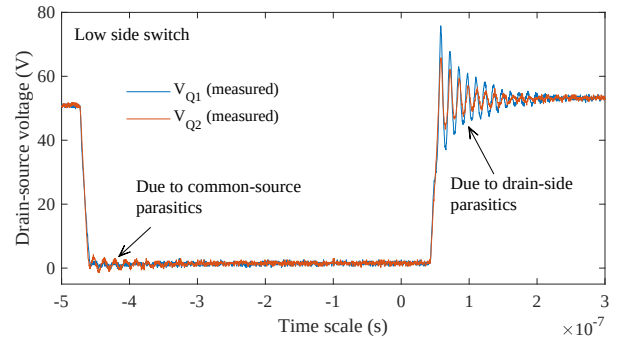
The experiment results were obtained for identical and non-identical components. The V_{th} and R_{on} of the identical components were in the ranges of 1.17–1.3 V and 50–70 mΩ respectively while non-identical components were in 1.17–1.44 V and 50–87 mΩ. No current sensors utilized in the circuit.

Figure 10(a) shows a comparison of the two identical GS66508T in parallel in the asymmetrical circuit. As seen in Fig. 10(b), the circuit parasitics caused the oscillations in voltages and currents. Due to more parasitic inductance in the drain-side of Q1, the amplitude of the Q1 oscillations during off-transition is higher than Q2. Further, the common-source inductance introduces oscillations during on-state.

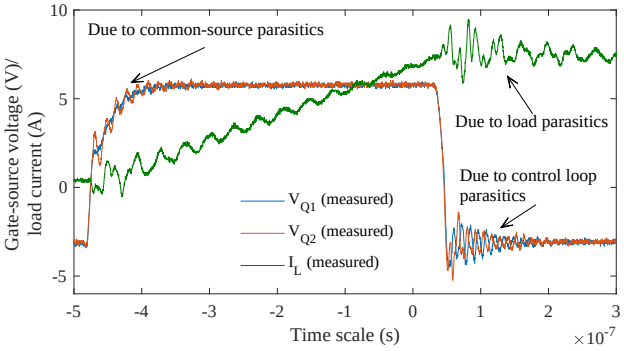
To predict the current via the parallel devices, the same technique in study [3] was applied (i.e. a Spice simulation model). The PCB parasitic components indicated in Fig. 11 were extracted using ANSYS Q3D software. These models remained the same for both identical and nonidentical components-based prototypes as only the GaN component been replaced from the PCB. In the simulations, the GaN device model was modified to adjust the electrical parameters to match the values obtained in parametric test results.

As depict in Fig. 10(c), the device close to the power supply draw more current at steady state but high oscillations can be seen during on-state due to the parasitic inductance in the control loop.

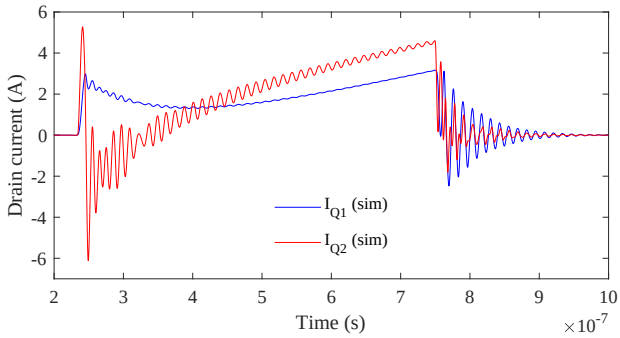
Later, a device in the switch (Q1 in Fig. 9(a)) was replaced with a non-identical device (V_{th} = 1.44 V and R_{on} = 87 mΩ). A comparison of simulation and experimental results are illustrated in Fig.s 12(a) and 12(b). These results indicate an achievement of an accurate simulation model. As seen in Fig. 12(c), the drain current of Q1 and Q2 are varied with respect to the identical component-based results. However, there is less impact on the drain currents at steady state and



(a)



(b)



(c)

Fig. 10. The experimental results of the asymmetrical circuit with identical components (a) drain–source voltages, (b) gate–source voltage and load current, and (c) prediction of the drain current using the simulation model.

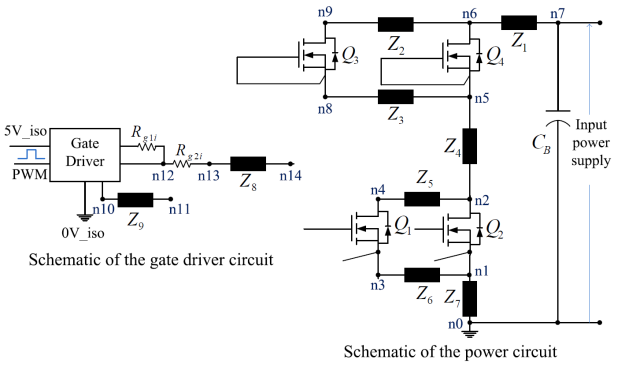


Fig. 11. A schematic of the PCB parasitic model.

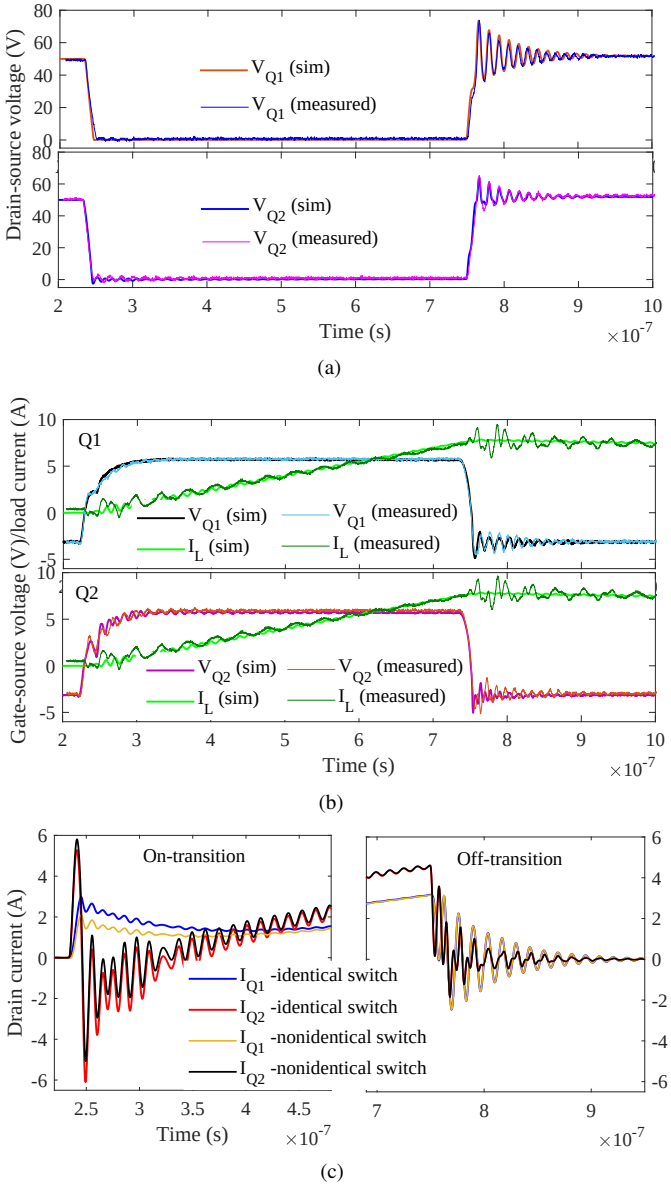


Fig. 12. A comparison: (a) and (b) experimental results of the asymmetrical circuit with non-identical components and (c) on and off transitions of the predicted drain currents with identical and non-identical components in parallel.

off-transient due to the electrical property variation. The high V_{th} device take longer time to switch-on hence more current flow through the low V_{th} device during on-transition.

V. Conclusion

In this study, both board parasitics and device electrical parameter discrepancies (i.e. threshold voltage in 10% and on-resistance in 25%) were investigated.

The experimental results and the simulations verified that the PCB parasitics affect the switching performance. The studies show that higher oscillations can be expected with increase of parasitic inductance in the board. The discrepancies in threshold voltages of parallel GaN HEMTs can leads to variation in current sharing among devices during on-transition. The effect of on-resistance on the switching transitions compared to threshold voltage is insignificant. The board level parasitics in these circuits are more prominent than that of the device discrepancies (V_{th} within 10% and R_{on} within 25%) on the switching characteristics in very fast transitions. This again proved that the GaN transistor-based designs are appropriate for circuit integration. To avoid the parasitic effect on the switching cell, very large integration can be implemented.

VI. Acknowledgment

A part of this work was funded by the French national program ”programme d’Investissements d’Avenir IRTNanoelec” ANR-10-AIRT-05. The authors would like to acknowledge the *ParaGaN* (Safran Tech - Paris Saclay) and the *GaNSiPSoC* (CEA-Leti, Grenoble) project teams for their numerous contributions.

References

[1] Lu, J., Bai, H., Brown, A., et al., ”Design consideration of gate driver circuits and PCB parasitic parameters of paralleled E-mode GaN HEMTs in zero-voltage-switching applications” in *2016 IEEE Applied Power Electronics Conference and Exposition*, Mar 2016, pp. 529–535.

[2] Y. Zhang, J.Li, and J.Wang, “Investigations on Driver and Layout for Paralleled GaN HEMTs in Low Voltage Application” IEEE IEEE Access, pp. 179134–179142 , Dec. 2019.

[3] T. Wickramasinghe, C. Buttay, C.Martin, et al., “An investigation of current distribution over four GaN HEMTs in parallel configurations,” IEEE The 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA 2019) , Oct. 2019.

[4] Billmann, ”Dimensioning of a proper coaxial shunt type”, presented at ECPE Workshop, Hamburg, Germany, Oct 17th, 2017.

[5] T. Wickramasinghe, B. Allard, C. Buttay, et al., “A Study on Shunt Resistor-based Current Measurements for Fast Switching GaN Devices” in Proc. IEEE Industrial Electronics Society vol. 1, pp. 1573–1578, Oct. 2019.

[6] G. Wang, J. Mookken, J. Rice, and M. Schupbach, “Dynamic and static behavior of packaged silicon carbide MOSFETs in paralleled applications” in Proc. Appl. Power Electron. Conf. Expo. (APEC), pp. 1478–1483, Mar 2014.