Characterization and modeling of 1200V – 100A N – channel 4H-SiC MOSFET

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ABSTRACT- The static characteristics of CREE 1200V/100A 4H-SiC MOSFET have been fully characterized at temperatures ranging from 0°C to 150°C. The distinct characteristics of high power SiC MOSFET compared with the silicon counterparts are analyzed and explained. A novel physics-based analytical model for SiC MOSFET has been developed by using the MAST language and simulated with SABER software to express the I-V characteristics. The influences of the geometry (short channel effects), channel mobility, temperature and the threshold voltage on transistor properties have been taken into account. The parameters used to define the device were extracted from measurements and datasheet.

Keywords—Device characterization, analytical model, modeling, simulation, SiC, MOSFET

1. INTRODUCTION

The silicon power MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) are the most widely used as switching devices in a broad range of power conversion applications. It can achieve a very high operating frequency (up to 1MHz), but it has failed to make serious inroads in the high voltage arena due to the increasing of on-state resistance with blocking voltages. Nonetheless the power MOSFETs provide high efficiency for applications for voltages below 200 V [1-3].

Based on innovative properties of wide band gap materials, silicon carbide (SiC) MOSFET offers advantages over conventional silicon devices such as enabling high system efficiency even at high temperatures, having excellent switching performances, simplifying the thermal design of power electronic systems. Emerging SiC power MOSFET has attracted tremendous attention for high-power applications to replace existing Si technology in the near future. However, before high performance SiC MOSFETs are realized, their performance limitations due to low mobility in the inversion layer must be understood and overcome [2, 4, 5]. Therefore, it is necessary to fully characterize the SiC MOSFET in order to evaluate its potential utilization, provide an important foundation for the behaviors and to compare it with its Si counterparts in systems. The characterizations results are then used to build an accurate model for the system design, power loss evaluation, and operation analysis of SiC power converters.

A lot of efforts have been carried out on development of SiC power MOSFET models in recent years. The existing Si models cannot be directly applied to SiC due to particular characteristics of SiC devices. Models presented in [3], [6] are accurate but they required many unknown parameters to be measured and determined prior to being implemented. Conversely, a simpler physical model of 4H-SiC devices was presented in [7] without explicitly accounting for the effects of traps on DC characteristics. In this work, an analytical model of the 4H-SiC MOSFET is developed, which is able to describe the on-state DC operating with the effects of short channel, the oxide–semiconductor interface traps and the parasitic resistances in a wide temperature range.

2. DEVICE CHARACTERIZATIONS

The static characterizations of the SiC MOSFET were measured and studied in terms of output characteristics (I_D-V_{DS}), transfer characteristics (I_D-V_{GS}), gate threshold voltage V_{TH} and on-state resistance $R_{DS(ON)}$. All these characterizations have also been performed under different temperatures from 0°C to 150 °C. At each temperature, the device was placed in a thermal chamber during 24 hours to allow the temperature stabilization.

2.1. Gate threshold voltage V_{TH}

The gate threshold voltage V_{TH} is essential to determine the on-state and the off-state of the MOSFET, which was defined as the voltage needed to produce a specified drain current (I_D). The threshold voltage was extracted at I_{DS} of 10 mA and observed at different temperatures.

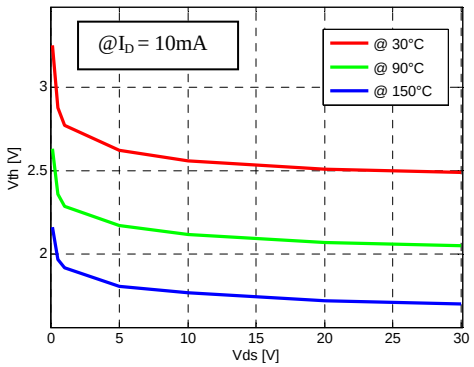

Fig. 1 Threshold voltage vs temperature and V_{DS}

As illustrated in Fig. 1, for a given voltage V_{DS}, the threshold voltage decreases with temperature. This behavior stems from the flat band voltage (V_{FB}), surface potential (ψ_S) and total charge in the depletion region (Q_D) dependency

towards the temperature. The calculation of threshold voltage is covered in many semiconductor literatures [1, 2, 8].

$$V_{TH} = V_{FB} + \psi_S - \frac{Q_D}{C_{ox}} \quad (1)$$

where C_{ox} is the oxide capacitance.

The more complete expression can be written [2]

$$V_{TH} = \frac{\Phi_{GS}}{q} - \frac{Q_F}{C_{ox}} - \frac{Q_{IT}}{C_{ox}} + 2\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) + \frac{\sqrt{4.q.\varepsilon_{SiC}.N_A.\psi_F}}{C_{ox}} \quad (2)$$

where ψ_F is the Fermi potential. The factor k is Boltzmann constant, T is temperature; ε is permittivity of semiconductor.

The work function Φ_{GS} declines due to the moving of Fermi level close to midgap with increasing of temperature. In other words, the voltage required to extract an electron from the Fermi energy level to the vacuum level reduces consequently. Moreover, charge in interface states (Q_{IT}) decreases in magnitude with increasing of temperature. A less negative Q_{IT} means a less positive threshold voltage. The density of fixed charge (Q_F) at the oxide/semiconductor interface is remaining. In general, V_{FB} the flat-band voltage decreases with temperature.

When the temperature increases, the band bending ($\psi_S = 2\psi_F$) also decreases related to the rapid raise of intrinsic carrier concentration (n_i). This is partially offset by factor k and the increasing of N_A with temperature. At the same time, depletion charge Q_D tends to decrease. These phenomena can explain the negative shift of V_{TH} with temperature in the experiments.

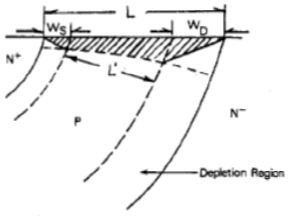

Fig. 2 PN juctions within P-substrate [9]

In addition, V_{DS} dependence on the threshold voltage was also observed. V_{TH} is found to shift negatively with decreasing drain voltage as the geometry dependence of V_{TH} in short channel MOS. The equation (1) assumes that the depletion charges under the gate only contribute to the vertical electric field, which is determined by V_{GS}. In short channel MOS, the PN junctions within the substrate formed by drain and source, begin to contribute greatly to the formation of the channel depletion region (as shown in Fig. 2). With PN junctions formed in the substrate, less gate charge density is needed to induce inversion in channel. The PN junction's widths (W_S, W_D) increase with V_{DS}, resulting in a lower V_{TH}. Thus, V_{DS}–dependent shift has been observed as Fig. 1.

2.2. On-state resistance $R_{DS(ON)}$

In power electronics applications, the MOS is employed as a switch. The $R_{DS(ON)}$ refers to the resistance between the drain and the source when the device is switched on.

In this work, the on-resistance was measured at I_{DS}=0A, in which the reversible current crossing the MOSFET was driven by a sine wave at zero average value with regard to two parameters, namely the gate voltage and the temperature. Frequency of the sinusoidal signal is at 100Hz, the amplitude of V_{DS} was kept at 100 mV to remain the operating point in the linear region (I-V curves as the straight lines).

$R_{DS(ON)}$ is in fact measured in the ohmic region where $R_{DS(ON)}$ is relatively constant with the definition.

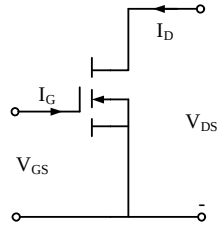

Fig. 3 Schematic of on-resistance test

For small V_{DS}, the effect of V_{DS} on threshold voltage and mobility is negligible, I_D can be calculated as

$$\begin{cases} I_D \cong \mu\frac{W}{L}.C_{ox}.(V_{GS} - V_{TH}).V_{CH} \\ V_{DS} = V_{CH} + I_D.R_D \end{cases} \quad (3)$$

V_{CH} is the voltage drop across the channel. R_D is the drain resistance. The R_{CH} is the channel resistance. The on resistance is considered equal to the ratio V_{DS}/I_D by the expression

$$R_{DS(ON)} = \left.\frac{\partial V_{DS}}{\partial I_D}\right|_{V_{GS}=const} = \frac{1}{k(V_{GS} - V_{TH})} + R_D = R_{CH} + R_D \quad (4)$$

where $k = \mu\frac{W}{L}.C_{ox}$ is the current gain factor.

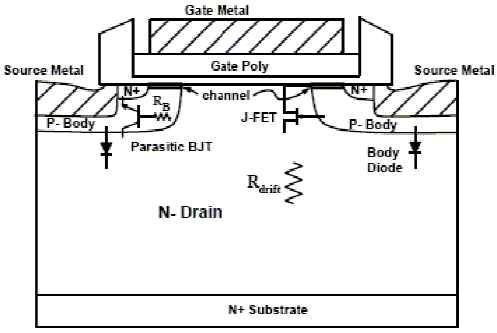

Fig. 4 Instrinic resistances of total on resistance VDMOS

As shown in Fig. 4, the electrons from the channel flow into the JFET region via the accumulation layer, and then spread into the N-drift region to the rest of the structure. The drain resistance of a MOSFET is considered expressed as the sum of several different resistances to be in series in the current path between the source and drain:

$$R_D = R_{ACC} + R_{JFET} + R_{DRIFT} \quad (6)$$

When a positive voltage is applied in gate, the accumulation layer formed underneath the gate. The R_{ACC} can be given as [1], [7]

$$R_{ACC} = \frac{0.6.L_{ACC}}{W.\mu_A.C_{ox}.(V_{GS} - V_{THA})} = \frac{0.6}{k_A.(V_{GS} - V_{THA})} \quad (7)$$

with $k_A = \mu_A\frac{W}{L_{ACC}}.C_{ox}$

0.6 is the coefficient accounting for the current spreading. L_{ACC} is the accumulation region length. Threshold voltage for the formation of the accumulation layer (V_{THA}) is lower than the V_{TH} (nominally V_{TH}). R_{ACC} is quite small in comparison with R_{CH} due to the mobility accumulation layer (μ_A) expected

to be higher than in an inversion layer [1]. However, SiC MOSFET with thin drift layer, the R_{ACC} is comparable contribution in the R_D. It was considered the dependence of the drain resistance on gate bias in the analytical expression.

R_{CH} has a negative temperature coefficient, while the other 3 components have a positive temperature coefficient. Due to the weight of resistances in $R_{DS(ON)}$, it represents a non-monotonic behavior with temperature for a given value of gate voltage.

$$\left.\frac{\partial R_{DS(ON)}}{\partial T}\right|_{V_{GS}=const} = \frac{\partial R_{CH}}{\partial T} + \frac{\partial R_D}{\partial T} \quad (8)$$

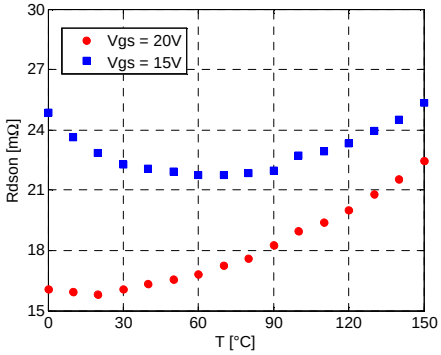

Fig. 5 On-resistance vs temperatures

The respective weight of each resistance in MOSFET $R_{DS(ON)}$ change with the gate voltage V_{GS}. For V_{GS} = 20V, R_{JFET}, R_{DRIFT} are dominant which make the whole on-resistance increase with temperature. When the gate bias voltage was applied at 15V, R_{CH} increases and becomes the dominant factors in $R_{DS(ON)}$ related to low mobility in channel of SiC MOS [10]. The on-resistance shows a negative temperature coefficient (NTC) for temperatures under 70°C. At higher temperature, R_{JFET} and R_{DRIFT} change faster than R_{CH} which leads to positive temperature coefficient as shown in Fig. 5.

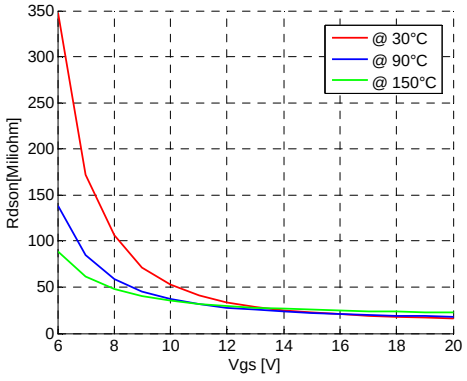

Fig. 6 On-resistance vs V_{GS}

It is obvious from Fig. 6 that the device always shows a NTC when it was biased lower than 14V at the temperatures ranging from 0°C to 150°C. This means the overall on-resistance of the SiC MOSFET becomes dominated by R_{CH}. SiC MOSFET requires gate-source voltage must be higher 14V to avoid thermal runaway and offer low on-resistance. The V_{GS} of 20V is suggested by the manufacturer to optimize performance. In system design aspects, the resistance temperature coefficient needs to be kept in mind when considering current sharing and lateral thermal stability.

2.3. Output characteristics

The output characteristics for the MOSFET are curves of drain current I_D as a function of drain-source voltage V_{DS} in the corresponding to a different value of gate-source voltage.

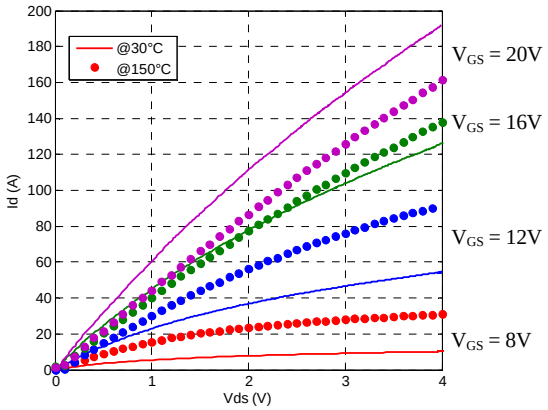

Fig. 7 Output characteristics vs V_{GS}

At a given V_{GS} above V_{TH}, the output characteristics are illustrated in Fig. 7 as a group of nearly straight lines. The unique behavior of SiC MOSFET $R_{DS(ON)}$ over temperature is not only determined by gate voltage as mentioned in section 2.2.

It can be observed from the output characteristics (see Fig. 7) that the drain current increases with the temperature when V_{GS} varying from 8V to 12V. This issue can be clarified. Indeed the R_{CH} plays an important role in the total on resistance at these gate bias (between 8V to 12V), leading to a decline of $R_{DS(ON)}$ with temperature due to the fact that $\frac{\partial R_{CH}}{\partial T} < 0$. As a result, the component tends to conduct more current when the temperature increases for 8V < V_{GS} < 12V. Conversely, it shows a negative temperature coefficient for V_{GS} = 20V because the weight of R_{CH} is no longer as important as it was for 8V < V_{GS} < 12V. As a result, the component has a tendency to conduct less current when temperature increases for V_{GS} = 20V.

Particularly, the device shows both negative and positive temperature coefficient of current depending on the operation point (see in Green curves in Fig. 7). This phenomenon can be explained by the case of V_{GS}=16V. The percentage of the R_D is slightly higher than R_{CH}. Undeniably, $R_{DS(ON)}$ has a positive temperature coefficient when V_{DS} is lower 2V. Then, the R_D is arguably reduced by increasing of V_{DS}; the effect of R_{CH} is momentous in the total on resistance, impacts on the decline in $R_{DS(ON)}$ over 2V.

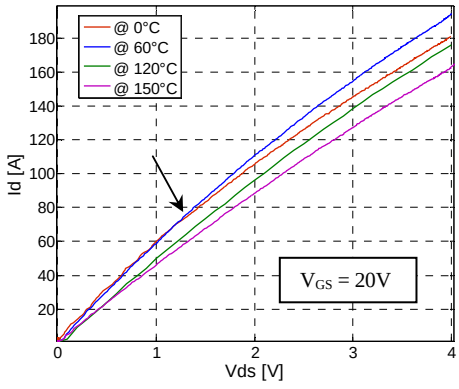

Fig. 8 Output characteristics at V_{GS} =20V

The dependence of drain resistance R_D on V_{DS} is illustrated in Fig. 8. The output characteristics of SiC MOSFET were observed in the same gate bias voltage (V_{GS} = 20V) at different temperature for comparison. The overall on-resistance of the SiC MOSFET is dominated by the drain resistance R_D (including R_{ACC}, R_{JFET}, R_{DRIFT}) for high gate voltage. At elevated temperatures (120°C, 150°C), R_D increases with temperature. However, at low temperatures (0°C, 60°C), R_D drops with an increase in V_{DS} faster than growing of it by temperature, resulting in consequent decrease of $R_{DS(ON)}$. Thus, drain current still raises with temperature despite of high gate biased.

2.4. *Transfer characteristics*

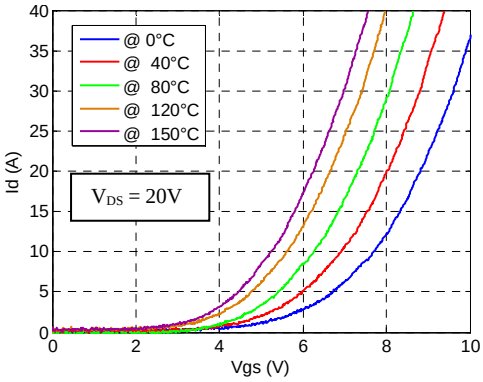

Fig. 9 Transfer charateritics I_D vs V_{GS} for different temperatures

The SiC MOSFET transfer curves are shown in Figure. 9, where drain current, I_D, is a function of gate voltage, V_{GS}, at fixed junction temperatures. The I_D increases with temperature at fixed gate bias voltage V_{GS} up to 10V. Therefore, the FET operates with possible thermal instability issue for V_{GS} inferior to 10V. It should be noted from the characteristics that the threshold voltage V_{TH} has a negative temperature coefficient as mentioned above.

As shown in Fig. 9, the device displays a shallow subthreshold slope, non-exponential turn on at threshold. It is due to the poor interface quality in the channel regions [5, 11]. At low positive gate voltage, most of charges are trapped by states. When gate voltage is increased, the Fermi level moves closer to the conduction band and more of the band-edge states become occupied. Consequently, all trap states are filled; additional charge can move freely in conduction band, leading to a gradual increasing of I_D.

3. ANALYTICAL SIC MODELING

There are several models of SiC MOSFET, however they often require either physics-based parameters (doping density, electron mobility, etc), or a proprietary tool for parameter extraction. The proposed model is none of them; it is only based on the conventional static data, and the use of MATLAB and Saber software's to fit the experimental curves.

Level 1 model, which is often referred to the Shichman Hodges model, employs fewer fitting parameters, it gives approximate results. It is useful for a quick and rough estimate of circuit performance and is normally adequate for analysis of power electronics. However, it is suitable for MOS device with a long channel. In this work, a modified version of level 1 model of Si MOS, which accurately portrays the 4H-SiC vertical DMOS power MOSFET electrical and thermal responses, has been developed.

The following equations describe the way the level 1 MOS model calculates the drain current, I_D

Cut-off region ($V_{GS}<V_{TH}$)

$$I_D = 0 \quad (9)$$

Ohmic region (on-state): $V_{GS} > V_{TH}$ and $V_{DS} \le (V_{GS} - V_{TH})$

$$I_D = \mu.\frac{W}{L}.C_{ox}.(V_{GS} - V_{TH} - \frac{V_{DS}}{2}).V_{DS} \qquad (10)$$

Saturation region (on-state): $V_{GS}>V_{TH}$ and $V_{DS} \ge (V_{GS} - V_{TH})$

$$I_{Dsat} = \frac{1}{2}\mu.\frac{W}{L}.C_{ox}.(V_{GS} - V_{TH})^2.(1+\lambda.V_{DS}) \qquad (11)$$

where L is the channel length; W is the width of the transistor; C_{ox} is the oxide capacitance and μ is the channel mobility. λ represents the channel length modulation factor.

3.1. *Parameters and extractions*

The nonlinear optimization method in MATLAB was applied to fit the models to the experiments and extract parameters. This method presents some advantages such as consistent determination the whole model parameters and reducing the effects of noise on experimental data based.

3.1.1. *Threshold voltage*

In short channel MOS, the formation of PN junctions in the substrate reduces gate charge density to induce inversion in channel. This means the depletion charge can be considered to be controlled by the V_{GS} and V_{DS}. Therefore, the dependence of V_{DS} on the threshold voltage was investigated as

$$V_{TH} = \frac{\Phi_{GS}}{q} - \frac{Q_F}{C_{ox}} - \frac{Q_{IT}}{C_{ox}} + 2\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) + \frac{\sqrt{4.q.\varepsilon_S.N_A.\psi_F}}{C_{ox}}.[1 - f(V_{DS})] \quad (12)$$

$$V_{TH} = V_{TH1} + V_{TH2}(V_{DS}) \quad (13)$$

The drain source voltage-dependent factor is now included in the prediction of the gate threshold voltage in the equation (1). The threshold voltage model is proposed for the simulation

$$V_{TH} = V_{TH1} + V_{TH2}.(V_{DS})^{kv} \quad (14)$$

The model is able to reproduce the threshold voltage measured at particular temperatures with good agreement.

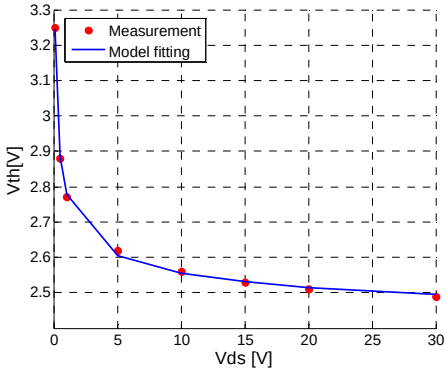

Fig. 10 Threshold voltage vs V_{DS} at 30°C, I_D = 10mA

The threshold is measured in the temperature range 0°C-150°C to investigate the performance as a function of temperature. The alteration with temperature of the three terms in (3) is dissimilar. Thus, threshold temperature coefficient MOSFET was modeled to decrease by the non-linear function with increasing temperature

$$V_{TH(V_{DS},T)} = V_{TH1}.e^{kt1.T} + V_{TH2}.e^{kt2.T}.(V_{DS})^{kv} \quad (15)$$

3.1.2. $R_{DS(ON)}$

The on-resistance $R_{DS(ON)}$ is either typically given in the datasheet or can be calculated from the output characteristic curve. In on resistance experiments, it was measured with a small sinusoidal signal of V_{DS} to remain the device in ohmic region.

By this way, measured $R_{DS(ON)}$ corresponds to the inverse of the slope at a specific I_D = 0A. The on resistance is considered as the function of gate bias by the expression

$$R_{DS(ON)} = \left.\frac{\partial V_{DS}}{\partial I_D}\right|_{V_{GS}=const} = R_{CH} + R_D \quad (16)$$

$$R_{DS(ON)} = \frac{1}{k(V_{GS} - V_{TH})} + \frac{1}{k_A(V_{GS} - V_{TH})} + R_{JFET} + R_{DRIFT} \quad (17)$$

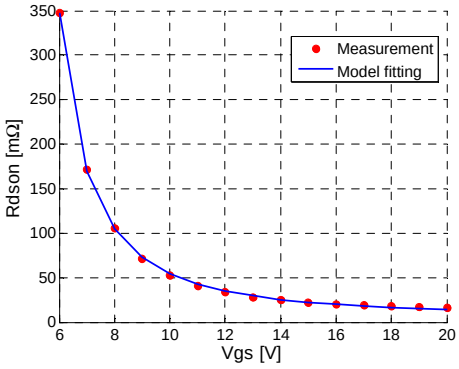

Fig. 11 On resistance vs V_{GS} at 30°C

As shown in Fig. 11, the model of $R_{DS(ON)}$ matches the measured data.

3.2. V_{DS} –dependent Drain Resistance

VDMOSFET is structured with a vertical JFET. Since the gate extends beyond the channel over the N- drain region, its surface becomes accumulated and becomes highly N+ for highly positive gates. This accumulation layer acts as the source of the vertical JFET. With respect to the shorted source and bulk, when a positive potential is applied to the drain electrode, the P-/N junction becomes reversed biased. The two symmetrically located depletion regions are pinching off the N-region and the current flow. This amounts to an addition of a parasitic JFET between the two adjacent P- base regions as shown in Fig. 12.

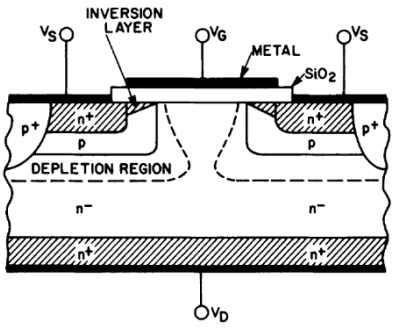

Fig. 12 Depeletion regions and JFET resistance in VDMOS

When the drain voltage is less than the gate voltage, the depletion region is negligible on the top of N- of the drain region due to the rich area of electrons (accumulation layer). As the drain voltage increases, the depletion region area around the P/N- region extends. The resistance JFET enhanced at higher drain voltage due to the pinch off action of depletion layers. Additionally, the length of the accumulation region (L_{ACC}) begins to decrease with the formation of a depletion layer under the gate [12]. The V_{DS}-dependent of R_D, can be expressed as:

$$R_D(V_{DS}) = R_{D0} + R_{D1}(1 - b.V_{DS}) \quad (18)$$

3.3. Carrier mobility

Inversion carrier mobility near threshold is half the bulk mobility in Si MOSFET, but it is only 5-10% in 4H-SiC due to high interface state density [2]. Electrons are trapped by interface states; a significant proportion of the electrons induced by the gate bias can not travel and contribute to the drain current. In reference [13], it was shown that trap saturation was observed and free carrier concentration keeps increasing with gate voltage. Moreover, carrier mobility in inversion layer SiC MOS is limited by several scattering mechanisms. In other words, the electrons mobility in the channel is not constant, it is a function of the vertical electric field (E_x) which is controlled by gate bias.

For increasing temperature, electrons trapped in interface state are emitted and more free carriers are available in MOS channel, resulting in a reduction of the channel resistance at high temperature.

When the channel length is shortened, the electric field along the channel increases. The lateral field (E_y) becomes high so that its influence on the carrier transport cannot be ignored. The electron drift velocity in the channel at low electric fields is proportional to the field, but at high field, the drift velocity tends to saturate. E_y = dV(y)/dy and V(y) increase with y, so the carrier velocity in non-saturation region at point y can be modeled as

$$v_{(y)} = \mu_n . \frac{\frac{dV_{(y)}}{dy}}{1 + \frac{1}{E_C}.\frac{dV_{(y)}}{dy}} \quad (19)$$

The expression of the current corrected for the velocity saturation becomes

$$I_D = \frac{1}{1 + \frac{V_{ch}}{L.E_C}} \frac{W}{L}.\mu_{no}(V_{GS},T).C_{ox}.\left[V_{GS} - V_{TH}(T,V_{DS}) - \frac{V_{ch}}{2}\right].V_{ch} \quad (20)$$

$$I_D = \frac{1}{1 + \theta.V_{ch}} \frac{W}{L}.\mu_{no}(V_{GS},T).C_{ox}.\left[V_{GS} - V_{TH}(T,V_{DS}) - \frac{V_{ch}}{2}\right].V_{ch} \quad (21)$$

where $\theta = \frac{1}{L.E_C}$ is θ the mobility degradation coefficient, E_C is critical electric field at which carriers become velocity saturated.

3.4. Premature saturation factor

The saturation voltage for a long-channel device was calculated assuming that the inversion charge density $Q_{IL(y)}$ was totally depleted ($Q_{IL(L)}$ = 0), the so called pinch-off condition. The conventional definition of saturation voltage $V_{DSsat} = V_{GS} - V_{TH}$ is obtained with $Q_{IL(L)}$ = 0. However, this classical condition for pinch-off is not realistic for short-channel devices. This is because the carriers reach velocity saturation even before the pinch-off conditions are fulfilled.

In reality the operating conditions that lead to pinch-off in short channel devices are not easy to define, especially with SiC MOSFET

$$V_{DSsat} = a.(V_{GS} - V_{TH}) \quad (22)$$

3.5. *Channel length modulation*

Typically, the current I_{Dsat} is independent of V_{DS}. However, in reality the shortening of the channel length involves a slight ascent of the current at high voltages. A small increase in I_{DSsat} does occur due to a phenomenon known as channel-length modulation λ as the equation.

$$I_{Dsat} = \frac{1}{2}\frac{W}{L}.\mu_{no}(V_{GS},T).C_{ox}.[V_{GS} - V_{TH}(T)]^2.(1+\lambda V_{ch}) \quad (23)$$

3.6. *Alpha factor*

For large series manufactured power devices, this equation (14) is not very satisfactory, which is not considered the effect of a depletion zone formed below the channel. This zone extends while the channel is narrowing. An expression of the current–voltage characteristics in consideration of the depletion charge can be described as [14]. C_D is the capacitance of the depletion region, with $\alpha = 1 + \frac{C_D}{C_{ox}}$

$$I_D = \frac{1}{1+\theta.V_{ch}}\frac{W}{L}.\mu_{no}(V_{GS},T).C_{ox}.\left[V_{GS} - V_{TH}(T,V_{DS}) - \alpha.\frac{V_{ch}}{2}\right].V_{ch} \quad (24)$$

3.7. *Model validation*

The following equations were implemented to depict the drain current depending on the operation regimes of the component.

$$\begin{cases} I_D = \dfrac{\mu_{no}(V_{GS})}{1+\theta.V_{ch}}.\dfrac{W}{L}.C_{ox}.(V_{GS} - V_{TH} - \alpha\dfrac{V_{ch}}{2}).V_{ch} \\ \text{when } V_{DS} \le a.(V_{GS} - V_{TH}) \\ I_{Dsat} = \dfrac{1}{2}\dfrac{W}{L}.\mu_{no}(V_{GS}).C_{ox}.(V_{GS} - V_{TH})^2.(1+\lambda V_{ch}) \\ \text{when } V_{DS} > a.(V_{GS} - V_{TH}) \end{cases} \quad (25)$$

$$V_{DS} = I_D.R_D(V_{DS},T,V_{GS}) + V_{ch}$$

$$k = C_{ox}.\mu_{no}(V_{GS},T).\frac{W}{L}$$

$$\theta = \frac{1}{L.E_C}$$

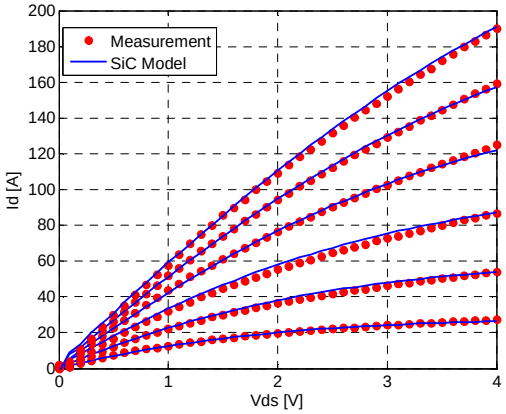

Fig. 13 The measured and simulated output characteristics at 30°C

The on-state resistance and threshold voltage have been extracted from experiment correspondingly. Based on the SiC MOSFET model developed, the I-V (the output and transfer) characteristics have been simulated and compared to the measured data at multiple temperatures.

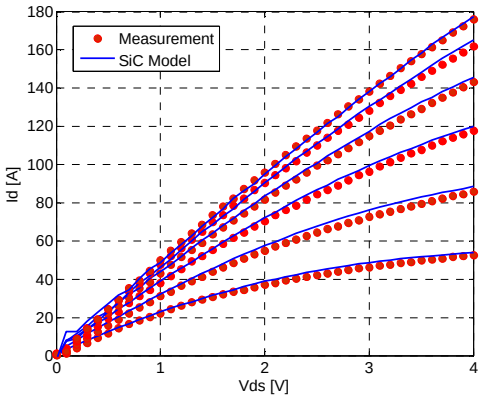

Fig. 14 The measured and simulated output characteristics at 120°C

The output characteristics are compared at different gate voltages (curves from bottom to top, V_{GS} varying from 10 V to 20 V, for each 2V, respectively) as illustrated in Fig. 13 (at 30°C) and Fig. 14 (at 120°C). The transfer curves have also been compared to experimental results at different temperatures in Fig. 15. As shown in the figures, the simulation results have good agreement with the experimental results at different operating conditions.

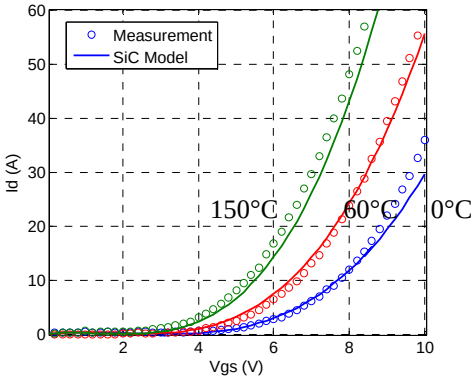

Fig.15 The measured and simulated transfer characteristics at V_{DS}=20V

4. CONCLUSIONS

An analytical model of the 4H-SiC vertical DMOSFET was developed to represent the forward DC current–voltage, which is based on physical considerations. The parameters were extracted from experimental tests. The trend of the model behavior is in good agreement.

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